Design and Implementation of A Signal Generator By Using Direct Digital Synthesis Technique

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Abstract

A PIC microcontroller is a main processor to generate four types of waveforms. This device has two channels output which not only provides user's editable waveform (sine, square, triangular, sawtooth etc) but also indicates user's frequency. The waveform synthesis is based on the Direct Digital Synthesis (DDS) technique to provide high stability and accuracy. The synthesized digital values at the port of the microcontroller are converted to an analog waveform by an 8-bit DAC. This signal generator can generate Sine, Square, Triangle and Sawtooth waveforms. It can operate standalone or with a personal computer (PC). A dot-matrix LCD is used to display the information about the waveform and the frequency selection. The type of waveform and the frequency selection can be selected from the embedded keypad or PC. The waveform table can be uploaded from the PC to the generator. The generator stores the received waveform table in the FLASH memory and uses it to generate waveform.

Key words: PIC, DDS, LCD, PC, FLASH, DAC

1. Introduction

In electronics, the signal generators are of great use in testing, designing and troubleshooting. The signal generators may be audio signal generators or radio signal generators. They may also be analog or digital. The circuit can be constructed by controlling PIC16F877-20P, 20MHz microcontroller from Microchip Corporation. It is over-clocked to 24 MHz by a clock generator, to get the sampling rate as fast as possible. The advantage of using microcontroller is that it is only a single chip to which we can program. This circuit has two main functions: the signal generation and production of the required frequency and waveform. It can operate by using a Direct Digital Synthesis (DDS) technique to create very accurate signals.

The DDS signal generator has four kinds of wave table in a FLASH memory, and produces wave patterns at frequency ranging from 1Hz to 10 kHz by 1Hz step. The DDS consists of four components; a phase accumulator, a memory, a digital-to-analog converter (DAC) and active low pass filter. The phase accumulator calculates the phase on each clock time and determines the memory address to read, which contains waveform table. The digital data read periodically from the memory address are converted into analog signal by the DAC. The final waveform is provided through an active low pass filter (LPF), which rejects the higher frequency components due to the transient change of the output voltage.

2. Background Theory

Direct-digital synthesizer (DDS) is an electronic device which generates accurate waveform of any kind. DDS is a type of frequency synthesizer used for creating arbitrary waveform a single, fixed-frequency reference clock. In a DDS, process for constructing a signal is almost entirely digitized. DDS technique works not as you would expect, by stepping sequentially through a table of waveform values at a variable rate, but instead uses a fixed very high frequency sampling rate, and a user controlled step size to address the table. The stability, accuracy and spectral purity of the output directly depend on the performance of the input reference. DDS can be a very useful device to generate waveforms.

In direct digital synthesis (DDS) technique, signal is generated in the form of a series of digital numbers and is converted into analogue by using a digital-to-analog converter (DAC). The output of the system is directly proportional to the frequency setting word.

Direct digital synthesis (DDS) technique for using digital data processing blocks as a means to generate a frequency and phase-tunable output signal referenced to a fixed-frequency precision clock source. In essence, the reference clock frequency is "divided down" in DDS architecture by the scaling factor set forth in a programmable binary tuning word. The tuning word is typically 24-48 bits long which enable a DDS implementation to provide superior output frequency tuning resolution.

A major advantage of a direct digital synthesizer (DDS) is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital processor control.

3. The Proposed Direct Digital Synthesis System Overview

The signal generator circuit constructed in this work can be expressed in the form of a block diagram as shown in Figure 1. PIC microcontroller is a main processor in this circuit. The waveform synthesis is based on the Direct Digital Synthesis (DDS) technique.

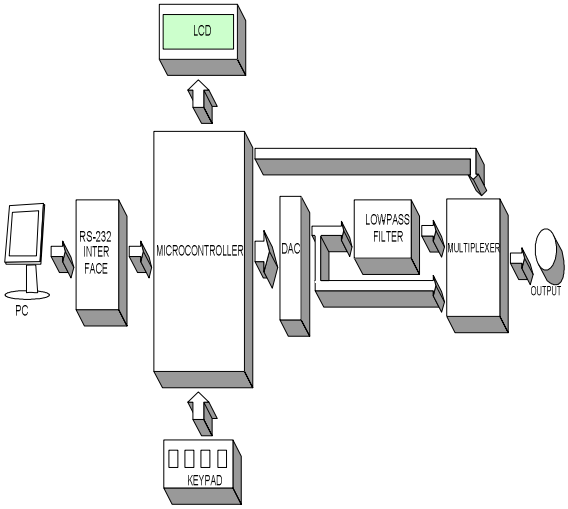

Figure 1. System Block Diagram of the Signal Generator

The synthesized digital values at the port of the microcontroller are converted to an analog waveform by a simple 8-bit R2R resistive ladder DAC. A 16x1 dot-matrix LCD is used to display the information about the waveform and the frequency selection. The type of waveform and the frequency selection can be selected from embedded keypad or from the PC.

The signal generator is constructed to be able to generate four types of waveforms: sine, square, triangle and sawtooth waveforms. The user defined waveform table can be uploaded from the PC to the generator. The generator stores waveform table in the FLASH memory and generates waveforms. The maximum frequency of this signal generator is 100 kHz. It can be generated by this circuit. It mostly depends on the speed of the processor. The precision of the circuit will be affected by the precision of the frequency counter or the oscilloscope used to calibrate the circuit.

By using the microcontroller we can program to output the desired frequency and waveform. The task of the microcontroller is to poll the user input, display the output and program the signal generator.
In many signal generators, output meters are included in the equipment to adjust and maintain the output at standard levels over wide ranges of frequencies. When using the signal generator, the output test signal is connected to the circuit being tested. The progress of the test signal can then be tracked through the equipment by using electronic voltmeters or oscilloscopes. In many signal generators, calibrated networks of resistors, called attenuators, are provided. Attenuators are used in signal generators to regulate the voltage of the output signal.

4. Hardware Implementation Process

The microcontroller- based signal generator by using DDS technique is designed and built by both hardware and software controlled. The waveform and frequency selection are displayed on the LCD display system, R2R ladder DAC and other control unit part are involved as a hardware implementation. The whole reading and controlling is done by PIC software.

4.1. Microcontroller

The PIC16F877-20P 20MHz microcontroller from Microchip Corporation, U_1, is used as a main processing unit. It is over clocked to 24MHz by a clock generator, Y_1, to get the sampling rate as fast as possible. The circuit is tested carefully and found that it is running well with this 20% over clock condition.

RA0 to RA3 pins of U1 are configured as digital output pins to send data to 16x1 character dot matrix LCD (Liquid Crystal Display), LCD1,RB0 to RB3 pins of U1 are configured as digital input pins to sense user input key entries. RB0 is also used as external interrupt, INT, input. Internal pull-ups of PORTB pins are enable to maintain high level on PORTB pins without using external pull-up resistors. RE0 and RE1 pins of U1 are configured as digital output pins to control LCD1. The RE2 pin of U1 is configured as digital output pin to control CD4053BC, analog multiplexer/ demultiplexer, U3.

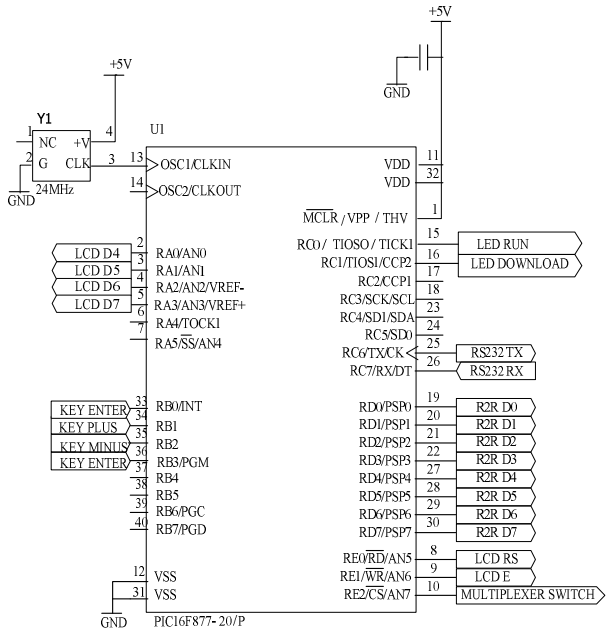

Figure 2. PIC 16F877 Microcontroller

All pins of PORTD of U1 are configured as digital output pins and which are connected to a R2R ladder DAC (Digital to Analog Converter) circuit. RC0 to RC1 pins of U1 are configured as digital output pins and are connected to two LEDs (Light Emitting Diode) to show the signal generator is running, RUN (LED1) and the data from the PC(personal computer) is receiving, DOWNLOAD (LED2). RC6 and RC7 pins are configured as transmit, TX, and receive, RX, pins of asynchronous serial communication interface (SCI). These pins are connected to voltage level converters.

4.2. Liquid Crystal Display (LCD)

The 1 line 16 characters LCD, LCD1, is used to display current waveform and frequency. It is also used to display waveform and frequency setting value during waveform and frequency changing time to see easily which digit is changing.

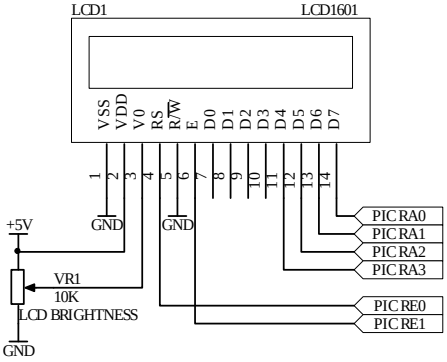

Figure 3. Liquid Crystal Display (LCD)

The LCD1 is configured as 4-bit data interface D4 to D7 pins are used for data inputs. R/$\overline{W}$ pin of LCD1 is pulled to ground because the LCD1 is used only for writing. The E pin of LCD1 is controlled by U1 to store the data. The RS pin of LCD1 is controlled by U1 to select whether the input data is command or data. V0 pin is used to adjust LCD brightness by using variable resistor, VR1.

4.3. Keypad

Four input keys S1 to S4 are used to enter user entries. Resistor R11, R16, R20 and R24 are series resistors used for Electrostatic Discharge (ESD) protection which are recommended by Microchip to use in keypad application. “ENTER” key is used to run and stop the signal generator.

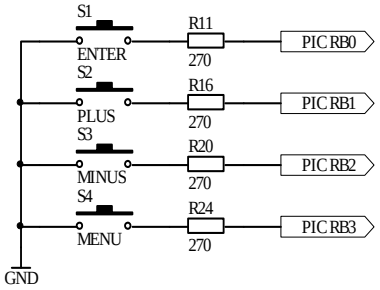

Figure 4. Keypad

It is also used to save the waveform and frequency value set by the user to the EEPROM (Electrically Programmable Read Only Memory) of U1 in setting mode. ‘PLUS’ and ‘MINUS’ keys are used in the setting mode of waveform and frequency to increase and decrease the current value displayed on the LCD1. ‘MENU’ key is used to enter the setting mode and escape from the setting mode.

4.4. R2R Ladder DAC

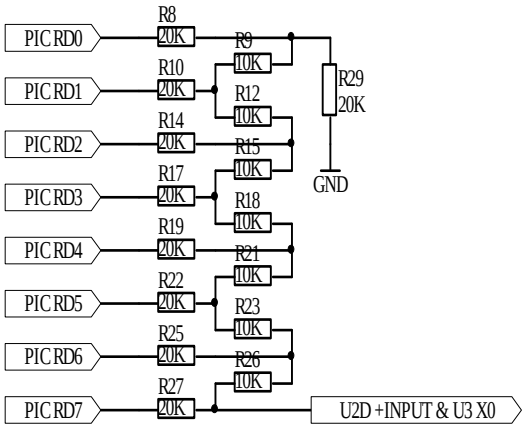

Figure 5. R2R Resistive Ladder Digital to Analog Converter

R8, R9, R10, R12, R14, R15, R17, R18, R19, R21, R22, R23, R25, R26, R27 and R29 are configured as an 8-bit R2R DAC. The outputs from PORTD of U1 are the digital inputs of the DAC and the node between R26 and R27 is the analog stepped output of the DAC. The output of the DAC is connected to two places, one is the X0 input of U3 and another one is the non-inverting input of U2D, the voltage level shifter, one part of TL084 operational amplifier, U2. The voltage level shifter, U2D, shifts the output 0 to 5V scale of the DAC output to approximately -3.25V to +3.25V scale outputs at the pin 14 of U2D.

4.5. RS232 Voltage Level Converter

Pin 2, RX pin, of the serial port at PC is used for receiving data from the signal generator and pin 3, TX pin, is used for transmitting data to the signal generator. RS-232 interface uses negative logic for transmitting and receiving data which means -3V to +12V voltage level is used to represent logic 0 and +3V to +12V voltage level is used to represent logic 1.

The data receiving is initiated by logic 1 to 0 transition (negative voltage level to positive level) at pin 2 of COM port and data transmitting is initiated by logic 1 to 0 transition (negative voltage level to positive voltage level) at pin 3 of COM port.

TX and RX pins of U1, however, use positive logic (0V for logic 0 and 5V for logic 1). Therefore, in idle state, TX pin of U1 is at 5V (logic 1) and pin 3 of COM port is at -12V (logic1).

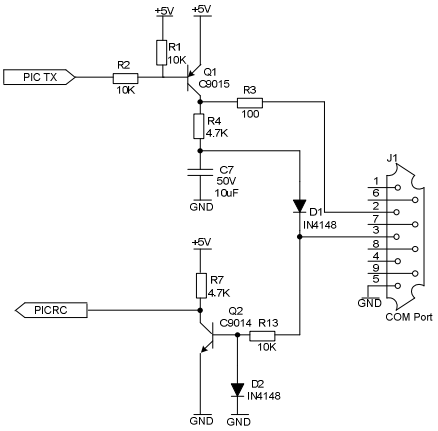

Figure 6. RS232 Voltage Level Shifter

If TX pin or U1 is 5V, it turns off the C9014 PNP transistor, Q1, and the negative voltage of pin 3 of COM port crosses diode D1 and appears at the collector of Q1. Therefore the negative voltage level (logic 1) appeared at pin 2 of COM port.

If pin 3 of COM port is logic 1 (negative voltage level), which turns off the C9014 NPN transistor Q2 and the RX pin of U1 becomes logic 1 (+5V).

If pin 3 of COM port is logic 0 (positive voltage level), which turns on Q2 and RX pin of U1 becomes logic 0 (0V). Diode D2 is used to prevent reverse base bias of Q2.

4.6. Level Shifter

The output wave from R2R DAC is in 0 to 5V range, which means the wave includes 5V peak-to peak AC signal and 2.5V DC part.

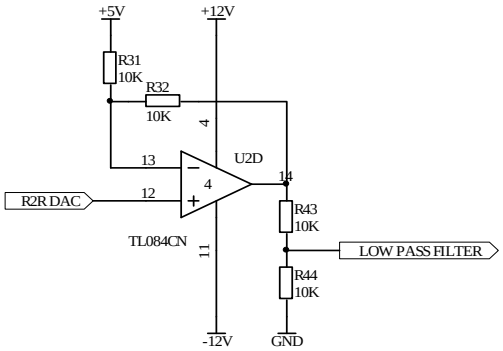

Figure7. Level Shifter

It is has to be filtered by active low pas filter, the DC part of the wave has be removed. In other word, the level of the wave has to shift to 0V offset (no DC part). U2D is configured to shift the wave signal to 0V offset.

It also amplifies the signal to 10V peak-to-peak. The output of U2D is divided by R43 and R44 to 5V peak-to-peak and is then fed to the active low pass filter.

4.7. Active Low Pass Filter

U2B and U2C are configured as cascading of two Sallen-Key second–order (two-pole) active low pass filters with critical frequency of about 300 KHz, which give -80dB/decade roll-off.

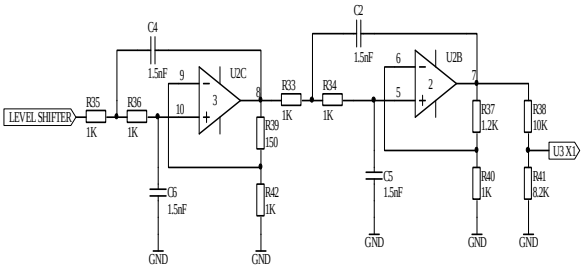

Figure 8. Fourth order Sallen-Key Active Low-Pass Filter

The critical frequency of each second-order filter can be determined by the value of capacitors and the resistors:

$$f_c = \frac{1}{2\pi\sqrt{R_A R_B C_A C_B}}$$

If $R_A = R_B$ and $C_A = C_B$,

$fc = 1/(2\pi RC)$

where $R = R_{35} = R_{36} = R_{33} = R_{34}$ and $C = C_4 = C_6 = C_2 = C_5$

if $f_c = 100$ kHz

$$100000 = \frac{1}{2\pi RC}$$

$$RC = \frac{1}{2\pi(100000)}$$

$RC = 1.59\ \mu s$

If $R = 1\ k\Omega$ is set then C = 1.5 nF

The R_{39} and R_{42}, R_{37} and R_{40} are selected by the damping factor. Since the damping factor of the fourth order low-pass filter in first stage is 1.848, the ratio of R_{39} and R_{42} is 0.152.

$$\frac{R_{39}}{R_{42}} = 0.152$$

If R_{39} is set 150 Ω

$$R_{42} = \frac{150}{0.15}$$

$R_{42} = 1\ k\Omega$

Thus R_{39} is 150 Ω then R_{42} is 1 kΩ.

The damping factor of the fourth order low-pass filter in second stage is 0.765, the ratio of R_{37} and R_{40} is 1.235.

$$\frac{R_{37}}{R_{40}} = 1.235$$

If R_{37} is set 1.2 kΩ

$$R_{40} = \frac{1.2k\Omega}{1.235}$$

$R_{40} = 1\ k\Omega$

Thus R_{37} is set 1.2 kΩ then R_{40} is 1 kΩ.

The input of low pass filter is taken from output of voltage level shifter and the output is divided by R_{38} and R_{41} to get approximately 5V peak-to-peak and fed to the multiplexer input X1.

4.8. Multiplexer and Output Amplifier

CD4053BC, U3, is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a signal-pole double-throw configuration. CD4053BC, U3 is used to multiplex between direct DAC output (no filter) and low-pass filter (with filter) output. VEE pin of U3 is used to connect to -12V supply to get full positive and negative voltage swing inputs and output. Control pin A is used to toggle inputs X0 and X1. The X output of U3 is fed to the non–inverting input of non-inverting amplifier U2A.

The purpose of output non-inverting amplifier is used for low output impedance. The voltage gain of U2A is derived from the following non-inverting amplifier formula:

$$A=1+R_f/R_i$$

Where $R_f = R_{28}$ and $R_i = R_{30}$.

Complete circuit diagram of the whole system is shown in figure 18.

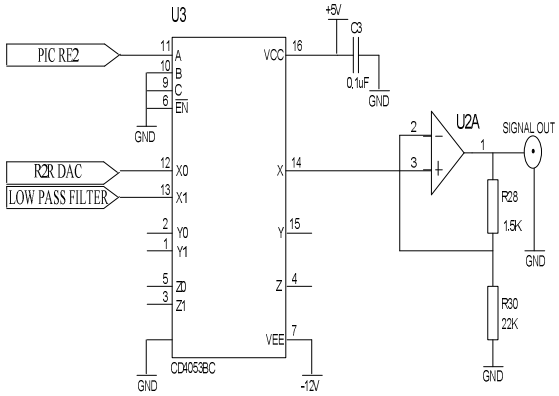

Figure 9. CD4053 Analog Multiplexer and Output Amplifier

4.9. Software Implementations

The firmware program for the microcontroller is compiled with the PICC Complier Tool suite version 8.02 from HI-TECH Software. The source code is written in the MPLAB IDE version 6.60 from Microchip Corporation. The PC terminal program is written and complied with Visual C#.NET from Visual Studio 2003.NET from Microsoft Corporation.

The PC program is used to upload the user defined wave table to the signal generator and to operate the signal generator from PC. The microcontroller uses RS-232 protocol to interface with the PC. The RS-232 protocol is configured as 2400bps transfer rate, 8 data bit, one stop bit and no parity.

Four push-button keys are used to enter user input and to control the signal generator. Low nibble pins of PORTB are configured as input port pins and PORTB internal weak pulled-up is enabled. The debouncing delay time and parallel pressing prevention are written in the firmware.

The microcontroller uses 4-bit data transfer mode to send data to the LCD. Since the LCD in this design is written only mode, the R/$\overline{W}$ is grounded. Only two control signals, RS and E, are needed for the LCD. These two signals are controlled by RE0 and RE1.

To get the highest sampling rate, 300 kHz, the microcontroller is over clocked by 24MHz clock generator. This signal generator uses 24-bit accumulator and 24-bit adder value. The adder value is obtained by the following equation.

$$\text{Adder} = \frac{F_{out}.2^{24}}{300\text{kHz}}$$

The accumulator is added by adder every sampling time and the most significant 8 bits of the accumulator value is used as the address of wave table.

The sine wave and user wave waveform table are stored in the flash memory of the microcontroller. The square, triangle and sawtooth waveform are mathematically generated by using the most significant 8 bits.

5. Overall Discussion

The aim of this research is to find an optimal signal generator by focusing on the circuit implementations of the DDS, by using a Microchip PIC16F877-20 microcontroller as a wave generator. Although the recommended clock for this microcontroller is 20MHz, in this research 24MHz clock is used to get maximum sampling speed (300 KHz). It is working well.

Three ICs, which are the circuit implementation of the DDS, used to design a signal generator. They are PIC16F877 microcontroller, TL084CN quad operational amplifier, and CD4053BC analog multiplexer. The microcontroller is used to get user input from push button keys, to calculate and generate the wave amplitude data for the DAC, to control the multiplexer, to send display data for the LCD module, and to interface with personal computer via serial port. The operational amplifier is used to remove dc component of the waveform and smoothing the sine waveform by forth-order filtering the sampling frequency. The multiplexer is used to multiplex the filtered and unfiltered wave.

5.1. Conclusion and Future Work

In this research, a PIC control signal generator circuit is constructed and tested. This generator can be used for testing or driving many circuits. The program can give out four waveforms with changeable frequency. The waveforms are sine, square, triangular and saw-tooth waveforms. The waveforms with different frequencies are generated by this circuit and outputs are checked on the oscilloscope. By checking with the oscilloscope, it is found that the frequency defined in the program and frequency measured with the oscilloscope is almost the same.

The circuit is interfaced with PIC and the operation of the circuit depends on the speed of the PIC. Successful digital signal processing requires the sampling frequency to be at least twice the highest signal frequency present. This is an important parameter of the practical limit being determined by the choice of software, and the characteristics of microcontroller. Microcontroller makes it very fast, running in a sampling frequency of 300 KHz.

The effect of digitally processing a 10 KHz waveforms (sine, square, triangle and sawtooth) using this system is shown in which the 3.3 µs sampling interval is clearly visible. Figure 15,16,17,18 show the outputs from filter. Figure 11, 12, 13 and 14 show the output from D-to-A in greater detail. Each step of the 10 KHz sine wave is composed of a sample of duration 3.3 µs, equivalent to the sampling rate of the digital system.

The signal generator is tested and photographed with KIKUSUI COM7060A 60 MHz Oscilloscope. This signal generator works best in the range from 1 to 10 KHz. Although it was designed for up to 100 KHz, the spur like noise occurs sometime at high frequencies due to switching noise of multiplexer.

5.2. Further Extensions

Higher frequency can be achieved by using DSP microcontrollers with high speed clock rates. Some features need to be implemented such as frequency sweeping, pulse and burst generating and wave amplitude controlling. The windows program would be looked well if the running waveform can be graphed.

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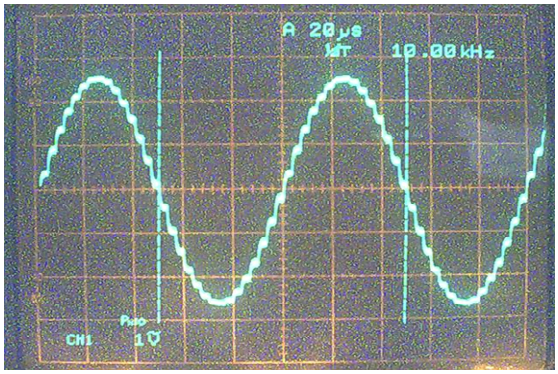

Figure 10. 10 KHz sine wave without filter

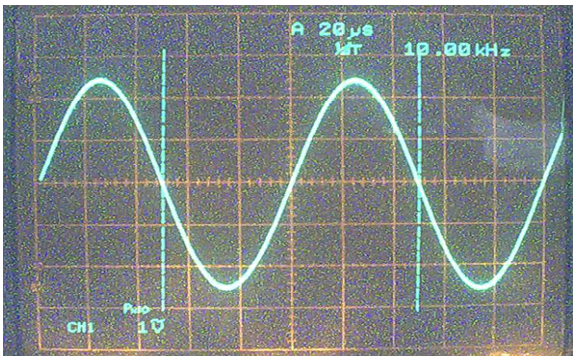

Figure 14. 10 kHz Sine Waveform with filter

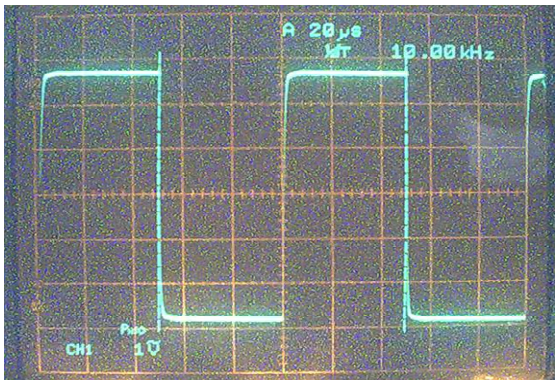

Figure 11.10 KHz square wave without filter

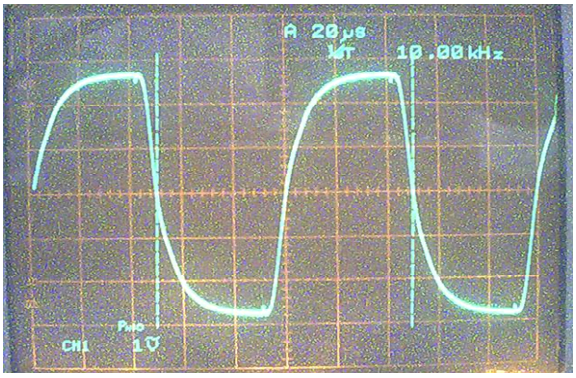

Figure 15. 10kHz **s**quare with filter

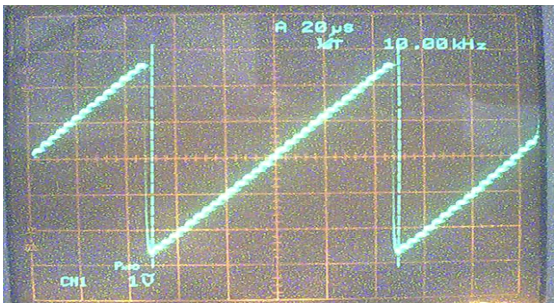

Figure 12. 10 KHz sawtooth wave without filter

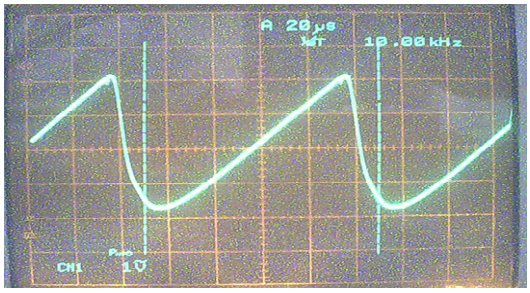

Figure 16. 10kHz sawtooth with filter

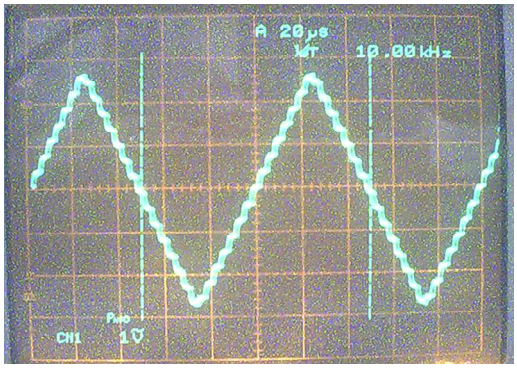

Figure 13. 10KHz Triangle wave without filter

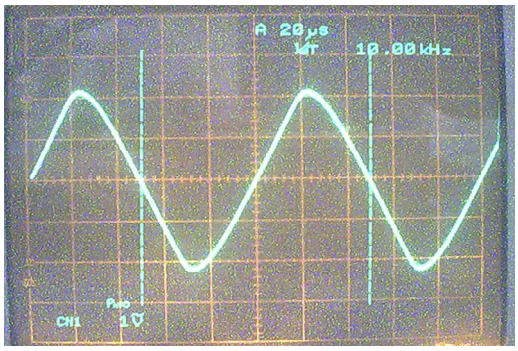

Figure 17. 10 kHz triangle wave with filter