STUDIES ON La DOPED Fe_2O_3 FERROELECTRIC THIN FILM CAPACITORS FOR MEMORY DEVICE APPLICATIONS

PhD DISSERTATION

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DEPARTMENT OF PHYSICS
UNIVERSITY OF YANGON
MYANMAR

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ABSTRACT

Ferroelectric memory devices of MFS design with La doped Fe_2O_3 thin films, with different concentrations from x = 0.02 mol% to 0.1 mole % are prepared by new liquid phase epitaxial route in which the substrate temperature was kept at 600°C for 1 hr. Current versus voltage characteristics, electric polarization versus electric field characteristics and transient current versus time characteristics of thin film capacitors are analysed. From detail analysis of the characteristics curves and their present results in this research work implies that the fabricated devices in all cases can be applied to nonvolatile memory devices. Particularly, ferroelectric field effect transistor (FeFET), ferroelectric memory diode (FMD) and ferroelectric random access memory (FeRAM) applications, have the bright future.

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CHAPTER I
INTRODUCTION

Ferroelectric is a phenomena which has discovered in 1921. The name refers to certain magnetic analogies, though it is somewhat misleading as it has no connection with iron (ferrun) at all. Ferroelectricity has also been called Seignette electricity , as Seignette or Rochelle Salt (RS) was the first material found to show ferroelectric properties such as a spontaneous polarization on cooling below the Curie point, ferroelectric domains and a ferroelectric hysteresis loop. A huge leap in the research on ferroelectric materials came in the 1950's, leading to the widespread use of barium titanate ($BaTiO_3$) based ceramics in capacitor applications and piezoelectric transducer devices. Since then, many other ferroelectric ceramics including lead titanate ($PbTiO_3$), lead zirconate titanate (PZT), lead Lanthanum zirconate titanate (PLZT), and relaxor ferroelectrics like lead magnesium niobate (PMN) have been developed and utilized for a variety of applications. The biggest use of ferroelectric ceramics have been in the areas such as dielectric ceramics for capacitor applications, ferroelectric thin films for non volatile memories, piezoelectric materials for medical ultrasound imaging and actuators, and electro-optic materials for data storage and displays.

Ferroelectric materials have (a)high dielectric constant (b)high piezoelectricity (c)relatively low dielectric loss (d)high electrical resistivity (e)moisture insensitivity (f)high electromechanical coupling (g)fairly high pyroelectric coefficients and, in some cases (h)good optical transparency and (i)high electro-optic coefficients which make them attractive for a variety of applications. However the most outstanding feature of a ferroelectric ceramic is its hysteresis loop observed in a plot of polarization vs. electric field which describes the non-linear polarization switching. The spontaneous alignment of electric dipoles

occurring in these materials is often associated with a crystallographic phase change.

Ferroelectricity can be observed in a relatively small class of dielectrics called ferroelectric materials. In a normal dielectric, upon the application of an electric field, positive and negative charges will be displaced from their original position - a concept which is characterized by the dipole moment or polarization. This polarization, or displacement, will vanish, however, when the electric field returns back to zero. In a ferroelectric material, on the other hand, there is a spontaneous polarization - a displacement which is inherent to the crystal structure of the material and does not disappear in the absence of the electric field. In addition, the direction of this polarization can be reversed or reoriented by applying an appropriate electric field.

The dipole moment, p, for two opposite point charges, is defined as p=Ql, where Q is the charge magnitude of each point charge and l is the spatial vector from the negative to the positive point charge. Applying this concept to a dipole distribution over a volume, polarization is defined as :

$$P(r) = \lim_{\Delta V \to 0} \left(\sum_{\Delta V} p \right) / (\Delta V) \qquad (1.1)$$

where delta-v is the volume over which the average is taken and **r** is the location vector.

The electric displacement, D, is related to the polarization through the linear expression:

$$D = \varepsilon E \qquad (1.2)$$

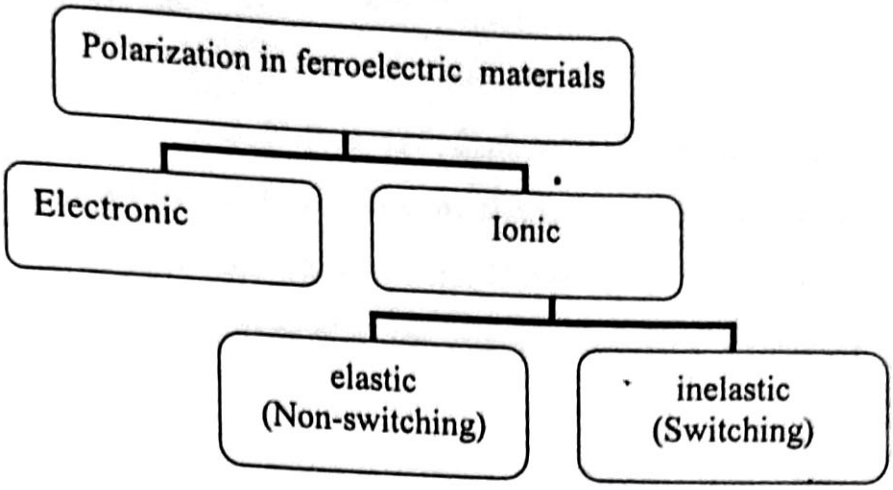
where the derived constant, epsilon, is the permittivity of free space.

The above equation states that the total charge on the capacitor is due to the superposition of two sources of charge: $\varepsilon_0 E$, which is the charge in the absence of dielectric, and P which is the extra charge introduced by a dielectric between the electrodes. For linear dielectrics, P is proportional to E, and hence, the above equation can be simplified and shown as:

$$D = \varepsilon_0 E + P \qquad (1.3)$$

where epsilon is the dielectric permittivity and can be interpreted as the capacitance of the unit-area, unit-thickness capacitor with dielectric. In ferroelectric materials, P is not merely a function of E; it also depends on the previous history of the material. In other words, the instantaneous voltage across an ferroelectric capacitor does not provide enough information to determine the capacitor charge.

Therefore, it is not possible to express D as a closed form function of E. However, as the polarization in ferroelectric materials is at least two or three orders of magnitude larger than $\varepsilon_0 E$, equation (1.3) can be approximated by: $D=P$. This equation implies that the total surface charge density on a capacitor with ferroelectric dielectric is equal, in magnitude, to the polarization. Polarization, in ferroelectric materials, can be broken into two fundamental components, namely; electronic and ionic polarization.



As their names suggest, electronic and ionic polarizations refer to the electronic cloud and ionic displacements with electric field, respectively. Ionic displacement, in turn, can be elastic (non-switching) or inelastic (switching). If the electric field is removed from the material, each electron cloud returns to its original position, and so does every ion which is displaced only slightly (elastic). However, those ions which are displaced through an inelastic mechanism keep their new positions, even after the removal of the electric field. In fact, it is these ions which make ferroelectric polarization much larger than their counterparts in normal dielectrics. For this reason, non-switching ionic polarization is also referred to as nonferroelectric ionic polarization.

If a sinusoidal electric field is applied to an ferroelectric material, after a few cycles, polarization will approach its steady-state condition. As larger electric fields are applied to an ferroelectric material, domains favorably oriented with respect to the field direction grow at the expense of other domains. This process continues with increasing electric field until the least favorably oriented domains switch to the polar direction most nearly coinciding with the electric field direction. When no further domain reorientation can occur, the P versus E response usually becomes linear. If the linear response is extrapolated to the

polarization axis (E=0), the polarization value at the intersection is designated as the saturation polarization P_{sat}.

The magnitude of polarization at E=0 is called remanent polarization and it is shown by P_r in the hysteresis loop. If no domains change direction while removing the electric field, P_r and P_{sat} would be the same. However, mechanical boundary conditions normally impose direction changes in some domains, causing P_r to be less than P_{sat}.

The coercive field, E_c, is defined as the horizontal intercept of the hysteresis loop or the field at which the net polarization becomes zero. In a single domain crystal, Ec can be interpreted as the field at which the polarization switches from one state to another. In a multi-domain crystal, however, E_c will lose its interpretation, as there is no single field at which all domains can switch.

In linear dielectrics, permittivity is defined as the ratio of electric displacement to electric field. In ferroelectric materials, which are nonlinear, two types of permittivity can be defined, namely small-signal and differential permittivity. The former, denoted as epsilon, is defined as the incremental change in electric displacement per unit electric field when the magnitude of the measuring field is very small compared to the coercive electric field. Macroscopically, epsilon is found by measuring the capacitance. The units of permittivity are coulombs/volt-meter. The measuring field or voltage must be kept small to prevent ferroelectric domain reorientation from contributing to this type of permittivity. In other words, only electronic and nonswitching polarizations contribute to small signal permittivity. Differential permittivity is defined as the slope of the hysteresis loop (electrical displacement versus electric field) at any point. The differential permittivity is partly affected by the inelastic polarization and therefore, is different from the small signal permittivity [1-6].

1.1 Ferroelectric Memory Design for Reliability

The most common ferroelectric semiconductor memory cells use a ferroelectric capacitor in series with an access transistor, similar to that used in a DRAM. For ferroelectric memories designed for hi-rel environments, two of these cells are used per bit, one programmed to the true logic state and the other programmed to the complement logic state. Differential sensing of pairs of cells provides larger margin for hi-rel applications than sensing the switching current of a single cell and comparing it to that of a reference cell.

The ferroelectric material used for the dielectric in these capacitors has the property that internal electric dipoles can exist in two states. Depending on the polarization state of these dipoles, either a logic "one" or logic "zero" is stored. During the first part of the read operation, an interrogation voltage is applied across the ferroelectric capacitor. If the polarization state of the capacitor changes, the resulting switching current charges the bit line. This current is much larger than the linear capacitance current that flows if the ferroelectric capacitor does not switch.

The first part of the read cycle just described is destructive during the read out. During the second part of the read cycle, the true state of the bit must be rewritten to restore the data. It is imperative that the restore portion of every read cycle is completed, even if the power is removed prematurely. Since the read cycle is very fast, typical under 100ns, adequate charge is stored on the internal nodes to complete the restore portion of the read cycle. Because every read is completed with a rewrite, endurance is based on the number of reads plus the number of writes. Ferroelectric materials that show very little or no fatigue with repeated read/write cycling, are ideal for use in memories designed for high-rel , high-endurance applications.

As with any memory device, ferroelectric memories for high-rel applications should be screened for defective memory cells. Ferroelectric memory cells that cannot be fully polarized and those that do not retain their polarization state for the specified retention period may occur. Special circuitry is used to allow weak writes and reads to be performed on every memory cell in the memory array. By detecting failing bits for weak writes and reads, chips with defective memory cells can be successfully screened using non-destructive electrical testing [7].

1.2 Ferroelectric Technology Reliability

Ferroelectric memory manufacturers use standard process qualification testing. This includes 1000 hour standard operating life and temperature testing. Thermal shock over extended temperature ranges to several hundred cycles, and high humidity pressure cooker tests to over 100 hours, are also used. Endurance is measured by cycling the memory at extended temperatures. A simple technique for assessing endurance is to measure the lowest power supply voltage at which the device will operate after the cycling is completed. If the voltage is compared to the lowest operating voltage prior to read/write cycling, it can be determined if any fatigue has occurred.

During one ferroelectric memory process qualification, using a statistically significant sample size, no failures were observed for high temperature storage, thermal shock and pressure cookers tests. At the same time, only one failure was observed. This failure, observed during life testing, occurred at one of the longest operating times. As compared to EEPROM technology of similar memory density, the reliability of the ferroelectric technology was observed to be comparable or better.

As is typical with other integrated circuit memory, testing at high temperatures can accelerate retention failures in ferroelectric memory. Normal operating

temperature failure rates can then be projected by extrapolation. A properly designed retention test will also screen for data imprint. Imprint is the phenomena where a memory cell prefers to remain in a particular polarization state as the result of repeatedly being programmed to that same polarization state. Imprint can be determined by repeatedly programming memory cells to the same polarization state, followed by programming them once to the opposite state, and then testing their ability to remain in that opposite state. Imprint phenomena are observed to be minor in Stronium Barium Titanate ferroelectrics [8-9].

1.3 Radiation Hardness of Ferroelectric Technology

The radiation hardness of ferroelectric memory has been measured for total ionizing doses, neutron exposure, heavy ion exposure and proton irradiation. These results indicate that ferroelectric memory can be used in severe radiation environments. Because the ferroelectric memory storage element is inherently radiation resistant, the hardness of ferroelectric semiconductor memories is primarily limited to the hardness of the underlying CMOS technology.

Ferroelectric thin films which are used for the dielectrics of the storage capacitors in ferroelectric memories have been shown to be tolerant to total ionizing radiation doses up to 100 Mrad (Si) without loss of data. This amount of radiation is higher than most CMOS circuitry can tolerate. Therefore, ferroelectric memories intended for high total dose environments must use radiation hardened CMOS circuitry.

Ferroelectric memories use capacitors that are formed after the underlying CMOS transistors are fabricated and before interconnect metallization. These capacitors layers require oxygen anneals at temperatures greater than to 600°C. These capacitor layers require oxygen anneals at temperatures greater than to 600°C to form in the proper ferroelectric phase. It has been demonstrated that these anneals

have an insignificant effect on the total dose hardness of the CMOS circuitry. Passivation layers are required for stable ferroelectric capacitors. It has also been demonstrated that silicon nitride passivation steps do not significantly degrade the radiation hardness of the CMOS circuitry. Therefore, ferroelectric memories using CMOS circuitry can be designed by processed to withstand total dose in excess of 1Mrad (Si) [10].

1.4 Ferroelectric Thin Films for Nonvolatile Memory Applications

Ferroelectric random access memory (FeRAM) has shown much potential in replacing volatile dynamic random access memory (DRAM), the current choice for computer technology. FeRAM is nonvolatile, meaning that the charge stored upon the bit capacitor is stable, negating the need for an energy-intensive data refresh. Thus, for portable applications where energy is limited, FeRAM is attracting significant interest.

One reliability issue encountered with FeRAM is fatigue, which is defined as a loss of swtichable polarization, or signal strength, with repeated switching. Dynamic random access memory (DRAM) is commonly used is most of today's computer technology. However, it is volatile, meaning that is must have access to a power source at all times, and any data stored upon it must constantly be refreshed in order to maintain it. As ferroelectric random access memory (FeRAM) is nonvolatile, it does not need constant access to a power source, giving it an advantage over DRAM in terms of power conservation. The polarization charge translates to a one or zero stored on a computer memory's capacitor, which is made of a ferroelectric material sandwiched between two metal electrodes [11-12].

1.4.1 Capacitor

The basis of a dynamic RAM cell is a capacitor. They are also used for power-supply smoothing (or 'decoupling'). This is especially important in digital circuits where a digital device switching between states causes a sudden demand for current. Without sufficient local power supply decoupling, this current 'spike' cannot be supplied directly from the power supply due to the inductance of the connectors and so will cause a sharp drop in the power supply voltage near the switching device. This can cause other devices to malfunction resulting in hard to trace glitches [13].

1.4.2 Dynamic Random Access Memory

A type of semiconductor memory in which the information is stored in capacitors on a MOS integrated circuit. Typically each bit is stored as an amount of electrical charge in a storage cell consisting of a capacitor and a transistor. Due to leakage the capacitor discharges gradually and the memory cell loses the information. Therefore, to preserve the information, the memory has to be refreshed periodically. Despite this inconvenience, the DRAM is a very popular memory technology because of its high density and consequent low price.

To reduce the pin count, thereby helping miniaturization, DRAMs generally had a single data line which meant that a computer with an N bit wide data bus needed a 'bank' of (at least) NDRAM chips. In a bank, the address and control signals of all chips were common and the data line of each chip was connected to one of the data bus lines.

Beginning with the 256 kilobit DRAM, a tendency toward surface mount packaging arose and DRAMs with more than one data line appeared (e.g 64k x 4), reducing the number of chips per bank. This trend has continued and DRAM chips with up to 36 data lines are available today. Furthermore, together with surface

mount packages, memory manufacturers began to offer memory modules, where a bank of memory chips was preassembled on a little printed circuit board. Today, this is the preferred way to buy memory for workstations and personal computers.

DRAM bit cells are arranged on a chip in a grid of rows and columns where the number of rows and columns are usually a power of two. Often, but not always, the number of rows and columns is the same. A one megabit device would then have 1024x1024 memory cells. A single memory cell can be selected by a 10-bit row address and a 10-bit column address.

To access a memory cell, one entire row of cells is selected and its contents are transferred into an on-chip buffer. This discharges the storage capacitors in the bit cells. The desired bits are then read or written in the buffer. The (possibly altered) information is finally written back into the selected row, thereby refreshing all bits (recharging the capacitors) in the row.

To prevent data loss, all bit cells in the memory need to be refreshed periodically. This can be done by reading all rows in regular intervals. Most DRAMs since 1970 have been specified such that one of the rows needs to be refreshed at least every 15.625 microseconds. For a device with 1024 rows, a complete refresh of all rows would then take up to 16ms; in other words, each cell is guaranteed to hold the data for 16ms without refresh. Devices with more rows have accordingly longer retention times.

PSRAMs (Pseudo Static Random Access Memory) are essentially DRAMs with a built-in address multiplexor and refresh controller. This saves some system logic and makes the device look like a normal SRAM. This has been popular as a lower cost alternative for SRAM in embedded systems. It is not a complex SRAM substitute because it is sometimes busy when doing self-refresh, which can be

tedious. Nibble Mode DRAM can supply four successive bits on one data line by clocking the CAS \ line.

Page Mode DRAM is a standard DRAM where any number of accesses to the currently open row can be made while the RAS signal is kept active. Static Column DRAM is similar to Page Mode DRAM, but to access different bits in the open row, only the column address needs to be changed while the CAS \ signal stays active. The row buffer essentially behaves like SRAM. Extended Data Out DRAM (EDO DRAM) can continue to output data from one address while setting up a new address, for use in pipelined systems.

DRAM used for Video RAM (VRAM) has an additional long shift register that can be loaded from the row buffer. The shift register can be regarded as a second interface to the memory that can be operated in parallel to the normal interface. This is especially useful in frame buffers for CRT displays. These frame buffers generate a serial data stream that is sent to the CRT to modulate the electron beam. By using the shift register in the VRAM to generate this stream, the memory is available to the computer through the normal interface most of the time for updating the display data, thereby speeding up display data manipulations.

SDRAM (Synchronous DRAM) adds a separate clock signal to the control signals. It allows more complex state machines on the chip and high speed 'burst' access that clock a series of successive bits out (similar to the nibble mode). CDRAM (Cached DRAM) adds a separate static RAM array used for caching. It essentially combines main memory and cache memory in a single chip. The cache memory controller needs to be added externally.

RDRAM (Rambus DRAM) changes the system interface of DRAM completely. A byte-wide bus is used for address, data and command transfers. The bus operates

at very high speed: 500 million transfers per second. The chip operates synchronously with a 250 MHz clock. Data is transferred at both rising and falling edges of the clock. A system with signals at such frequencies must be very carefully designed, and the signals on the Rambus Channel use nonstandard signal levels, making it incompatible with standard system logic. These disadvantages are compensated by a very fast data transfer, especially for burst accesses to a block of successive locations [14-16].

1.4.3 Erasable Programmable Read-Only Memory

A type of storage device in which the data is determined by electrical charge stored in an isolated ("floating") MOS transistor gate. The isolation is good enough to retain the charge almost indefinitely (more than ten years) without an external power supply. The EPROM is programmed by "injecting" charge into the floating gate, using a technique based on the tunnel effect. This requires higher voltage than in normal operation (usually 12V-25V). The floating gate can be discharged by applying ultraviolet light to the chip's surface through a quartz window in the package, erasing the memory contents and allowing the chip to be reprogrammed [17].

1.4.4 Ferrite Core Memory

An early form of non-volatile storage built (by hand) from tiny rings of magnetisable material threaded onto very fine wire to form large (e.g 13 inches x 13 inches or more) rectangular arrays. Each core stored one bit of data. These were sandwiched between printed circuit boards. Set of wires ran horizontally and vertically and where a vertical and horizontal wire crossed, a core had both wires threaded through it.

A single core could be selected and magnetized by passing sufficient current through its horizontal and vertical wires. A core would retain its magnetization until it was re-magnetized. The two possible polarities of magnetization were used to represent the binary values zero and one.

A third 'sense' wire, passed through the core and, if the magnetization of the core was changed, a small pulse would be induced in the sense wire which could be detected and used to deduce the core's original state [18].

1.4.5 Ferroelectric Random Access Memory

FeRAM is a type of non-volatile read / write random access semiconductor memory. FeRAM combines the advantages of SRAM-writing is roughly as fast as reading, and EEPROM-non-volatile and in-circuit programmability. Current disadvantages are high cost and low density, but that many charge in the future. Density is currently at almost 32 kB on a chip, compared with 512 kB for SRAM, 1MB for EEPROM and 8 MB for DRAM.

A ferroelectric memory cell consists of a ferroelectric capacitor and a MOS transistor. Its construction is similar to the storage cell of a DRAM. The difference is in the dielectric properties of the material between the capacitor's electrodes. This material has a high dielectric constant and can be polarized by an electric field. The polarization remains until it gets reversed by an opposite electrical field. This makes the memory non-volatile.

Data is read by applying an electric field to the capacitor. If this switches the cell into the opposite state (flipping over the electrical dipoles in the ferroelectric material) then more charge is moved than if the cell was not flipped. This can be detected and amplified by sense amplifiers. Reading destroys the contents of a cell which must therefore be written back after a read. This is similar to the precharge

operation in DRAM, though it only needs to be done after a read rather than periodically as with DRAM refresh. In fact it is most like the operation of ferrite core memory.

FRAM has similar applications to EEPROM, but can be written mush faster. The simplicity of the memory cell promises high density devices which can compete with DRAM [19].

1.5 Basic Operation and Properties of Ferroelectric Memories

A ferroelectric crystal of the tetragonal perovskite structure has two polarization states . In lead titanate ($PbTiO_3$), for example, the Ti^{4+} ions occupy the centers of each cube; the Pb^{2+} ions are located at the corners; and O^{2-} ions are centered on each face of the undistorted lattice. In the distorted ferroelectric phase that is stable at room temperature, there is a net dipole (spontaneous polarization, P_s) of a few tens of microcoulombs per square centimeter produced primarily by the displacement up or down of the Ti^{4+} ions with respect to the other ions. In a crystal of $PbTiO_3$ that has not been specially prepared, we might expect to find regions in which the polarization is up and regions in which it is down, called "ferroelectric domains". However, if we apply a large electric field to the specimen, all the domains can be lined up in the same direction. More important for memory applications, we can switch the polarization of the entire crystal can be switched from up (+1) to down (0) by reversing the applied field.

In a large single crystal this would require voltages of several kilovolts, which would be impractical for a commercial device; but for a thin film of order 100 nm thick, it requires only a few volts. Thus the development of practical ferroelectric memories is closely linked with progress in thin film physics and engineering.

A basic characteristic of all ferroelectric material is the hysteretic behavior relating polarization P and applied field E_a. There is a nominal threshold (or coercive field E_c), above which the polarization changes sign. The two zero field values $\pm P_r$ are equally stable. Thus, no applied field or voltage is required to maintain the memory, which is why the device is termed "nonvolatile". This bistable operation may be contrasted with the operation of memories such as nematic, liquid-crystal display devices, which relax back to a single favored state if the applied voltage is interrupted, or with Si DRAMs, which require a "refresh" voltage many times per second to maintain their stored information.

The individual unit cells interact constructively with their neighbours to produce domains within the material. As the voltage is removed, the majority of the domains will remain poled in the direction of the capacitor. The compensating charge causes a hysteresis in the standard charge versus voltage plot of the capacitor as it is cycled through positive and negative voltage applications. From a digital point of view if a voltage is applied to a ferroelectric capacitor in a direction opposite of the previously applied voltage, remanent domains will switch, requiring compensating charge to flow onto the capacitor plates. If the field is applied in the direction of the remanent domains, no remanent switching takes place, no charge occurs in the compensating charge will flow into the capacitor. This property can be used by a properly designed external circuit to sense the last state of the capacitor or write a desired state into the capacitor. The remanent charge does not generate a detectable voltage on the capacitor after the removal of the applied field. In fact, unlike a DRAM capacitor, the plates of the ferroelectric capacitor can be shorted without affecting the remanent charge internally and the charge requires no refresh. All of the early work on ferroelectric memories involved a simple design scheme. In this prototypical row-and-column array architecture, there is a ferroelectric cell at the intersection of each metallized

row and column [or, in the parlance of computer engineers, at the intersection of each "word-line" (WL) and "bit-line" (BL)].

To write information in such a memory, short voltage pulses are applied along the rows and columns. Each voltage pulse is of value 0.5 V_s, where V_s is the nominal switching voltage, given by $V_s = E_c d$, where d is the film thickness. Unfortunately, such a simple row-and-column address scheme is impractical for ferroelectric memories. The reason is that real ferroelectrics do not exhibit well defined coercive fields or switching voltages; instead, E_c and V_s depend on the duration of the applied field, and on the history of the cell. In a typical ferroelectric the chances that a cell adjacent to the one being addressed will unintentionally also switch is 10^{-3} to 10^{-6}.

In a large memory this would produce an unacceptably large error rate in writing information into the memory. In the jargon of computer memory designs, this problem was referred to as a " half-select disturb pulse threshold", which means that half the V_s could unintentionally disturb, or switch stored data in a cell.

A better way to deal with the disturb problem is simply to circumvent it by designing around the problem, a more modern scheme is one in which each ferroelectric memory cell is electrically isolated from its neighbours by a pass-gate transistor. All modern ferroelectric RAMs use a variant of this transistorized array, typically either a six-transistor SRAM design or a more dense two-transistor DRAM layout.

A second problem associated with early research and development of ferroelectric memories is that they were fabricated from single crystal or ceramics. That

resulted in thick cells and consequently unacceptable large operating voltages for practical commercial devices [20-22].

1.6. Progress in Ferroelectric Memory Technology

Progress in ferroelectric memory technology must be reviewed in terms of system requirements and not in terms of universal specifications. Memory, while a simple word, has many connotations. We have semiconductor memories that are optimized for a variety of applications. These are static random access memories (SRAMs) that are optimized for high-speed applications including cache; dynamic RAMs (DRAMs) that are designed for computer storage and require continued circulation of data; and several nonvolatile memories ranging from read-only-memory (ROM), which is permanent to electrically erasable ROM (EEPPOM). The nonvolatile memory can be read either destructively (DRO) or nondestructively (NDRO).

A second major memory segment is the magnetic memories that are exemplified by random access memories such as magnetic core and plated wire; higher density memories such as magnetic bubbles and permalloy thin films; and permanent storage such as magnetic tape and discs. Optical memories form a third group. The new optical disc memory that is characterized by write once read many (WORM) operation and archival film storage are examples of this family.

For all type of memories, certain properties must be examined and specified by the system user. Some of the most important characteristics are described below with special emphasis on those characteristics that apply to ferroelectric memories. The capacity (or number of bits per chip) along with the read access and write access times are properties of importance in every memory. The operating and storage

temperature limits are important for many applications such as military and space. The power required for the memory For nonvolatile memories several other properties are usually mentioned. These are the retention (unpowered storage time), endurance (the number of read or erase and write cycles before the memory is lost), disturb effects such as read disturb (where reading a bit causes a change in retention or endurance) and pattern sensitivity (where reading a bit at one location can affect the storage at an adjacent location). These properties are of differing significance depending on whether the memory is DRO or NDRO [23-27].

1.7. Ferroelectric Application to Memories

Ferroelectric materials can be used in different ways in memory designs. The first use is a thin film of ferroelectric in a capacitor as a nonvolatile storage element using the hysteresis property of polarization versus voltage as the means of storing data. The high dielectric constant of ferroelectric materials can be exploited by using a thin film capacitor as the storage element in a DRAM in place of trench capacitors. Here, the hysteresis is not desirable, and the capacitor operates as a linear capacitor for charge storage. Another class of memory applications is the electrical write with optical read storage element. This takes into account the varying optical properties of ferroelectric thin film with polarization. Setting the polarization and using the birefringence of the film can allow for dense NDRO storage.

The advantages of thin film ferroelectric memories for nonvolatile storage are significant when compared to other technologies and have created a wide interest in this application. The first advantage is nonvolatility when combined with semiconductor processing, which leads to the potential of large capacity chips. Integration levels of 256 k-bits to 1 M-bit appear to be feasible in the near future.

For aerospace and military applications, the storage of data by polarization instead of electric charge gives a significant improvement in radiation resistance; particularly to charged particles such as cosmic rays which cause the so called single event upset (SEU) or soft errors. The immunity to SEU is of great value in space. Finally, ferroelectric memories offer the potential of low cost per bit particularly when compared to magnetic storage elements.

To understand how the nonvolatile ferroelectric memory works, we refer to Fig.1.1. which shows a typical hysteresis curve. If a positive voltage greater than the coercive voltage (V_c) is applied to the ferroelectric capacitor, then the film is polarized in the positive direction with a polarization value of P_s (or saturated polarization). Once the voltage is removed from the capacitor, the polarization relaxes slightly to the value P_r (called remanent polarization). We arbitrarily call this positive polarization a zero. If a negative voltage is applied to the ferroelectric film, the resulting polarization is in the negative direction at $-P_s$. This is called a one. Again, when the voltage is removed, the polarization relaxes to the value $-P_r$. Thus we have two stable stats at zero voltage which have been arbitrarily defined as zero and one. This is nonvolatile storage element since the data is present when voltage is removed.

To read this storage element, we apply a positive voltage to the capacitor. If the stored data were a zero, a small current equal to the increase in polarization from P_r to P_s is observed. If a one was stored, then the current is created by the change in polarization from $-P_r$ to P_s. The difference between these two currents is sensed to give the output from the memory. Obviously, the greater the difference between dP (1) and dP (0), the greater is the signal to noise ratio of the memory output. In a typical digital system, this signal to noise ratio must allow the determination of either one or zero to a probability of 0.999. The memory is destructively read since

all data are now in the zero state. If we had stored a one, it is required that we reverse the voltage and rewrite the negative polarization. This can be easily designed into the circuit.

The main emphasis is that read voltage is always in the same direction, the stored value is read as a low current (zero) or a high current (one), and the value of one must be rewritten after a read. The coercive voltage is defined as the value where the polarization reverses and the curve crosses the x-axis. A perfectly square hysteresis loop is the most desirable [28-30].

1.8. Present Generation of Ferroelectric Memories

At present, the ferroelectric prototype memories being produced in the United States involve either sputtered films or sol-gel deposition. Other techniques can be used in some special cases, but expensive techniques such as molecular beam epitaxy (MBE) are not required. Moreover, the device can be fabricated with deposition of the ferroelectric film as a postproduction step on a Si IC that has been fabricated up to the first metal layer (bottom electrode) in a standard CMOS production facility. The ferroelectric film, top electrode, passivation layers, and so on can be put down in a rather small production facility without the need to rerun the IC through the Si line; this eliminates any possible contamination of an Si IC wafer line by the metal ions in the ferroelectric and greatly decreases the capital investment in such a ferroelectric RAM production facility.

Historically, the present generation of ferroelectric RAMS traces its origin to a few key development steps. In 1967 Schubring *et al* at General Motors investigated the properties of KNO_3 switching films that were thermally deposited in a simple manner. In 1973 Rohrer found that KNO_3 films could be made

sufficiently thin to permit 5 V operation (CMOS-compatible) ; that their operating temperatures were greatly enhanced above the bulk values (the Curie temperature of the film T_c = 196°C at thickness d = 70 nm, versus T_c = 127°C in bulk); and that they exhibited excellent fatigue and retention characteristics. Rohrer fabricated raw arrays of order 1 kbit. Somewhat later Nakagawa *et al* pointed out the need to develop sputtering techniques for lead zirconate-titanate (PZT) thin film RAMs. Sputtered PZT is the basis for the ferroelectric 4-kbit RAM produced this year by Ramtron and TRW. Equally good PZT memories have been prepared by sol-gel deposition; this wet chemistry technique was pioneered by Payne at the University of Illinois and Dey *et al* at Arizona State University and is utilized by Krysalis in its ferroelectric RAMs. Other wet chemistry alternatives to standard sol-gel deposition have also been investigated for PZT, particularly processes involving soap-like precursors and xylene solvents developed by Vest and Xu at Purdue University. In addition to PZT, switching in sputtered lead germanate thin films has been reported by Volz *et al*. and barium bismuth titanate is known to be extraordinarily fast, with 1-ns switching speeds extrapolated. The materials requirements for the ferroelectric film chosen are relatively modest; in particular, because most ferroelectrics have a polarization that corresponds to about 100 times the switched charge of a Si DRAM of the same area, it is not necessary to choose a ferroelectric material with a large spontaneous polarization: 0.1 to 1.0 $\mu C/cm^2$ is sufficient. This permits many non-oxide crystals to be considered as cell materials, in addition to the ABO_3 perovskites favored at present. The integration of ferroelectric thin film arrays with CMOS Si integrated circuitry was first made by Mc Millan and his co-workers, an extremely important step in the development of commercially viable ferroelectric RAMs [31-34].

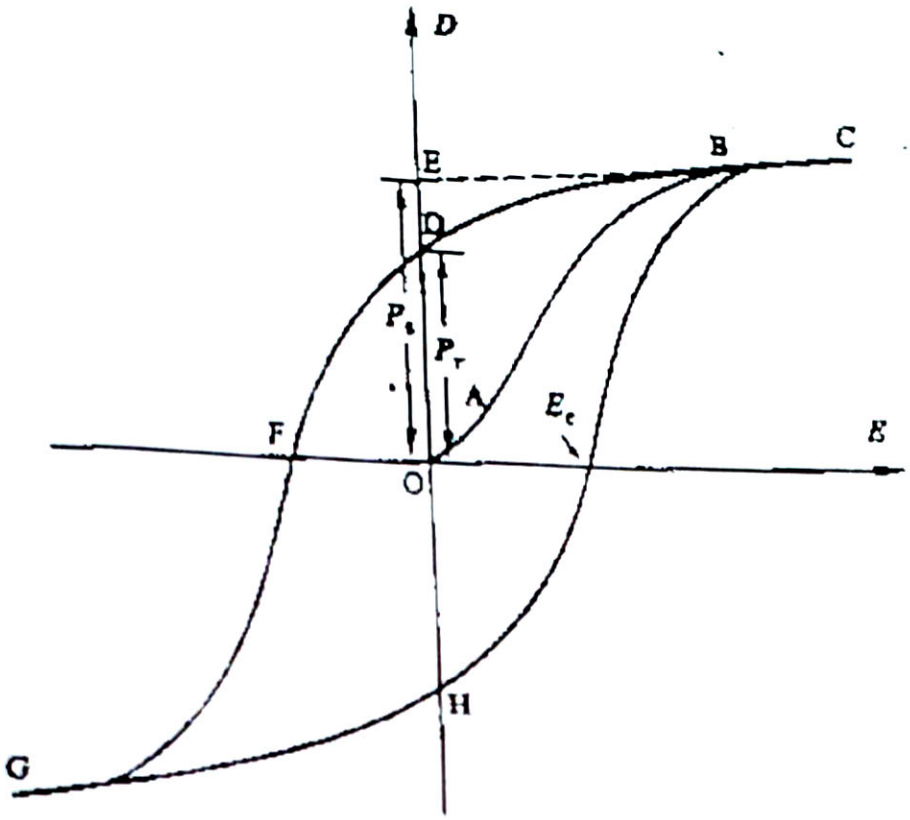


Fig 1.1 A Typical P-E Hysteresis Curve.

CHAPTER II

CHOICE OF SUBSTRATE AND MATERIALS SYSTEM FOR THE FABRICATION OF THIN FILMS

2.1 Silicon

Solid state electronics arises from the unique properties of silicon and germanium, each of which has four valence electrons and which form crystal lattices in which substituted atoms (dopants) can dramatically change the electrical properties. In solid state electronics, either pure silicon or germanium may be used as the intrinsic semiconductor which forms the starting point for fabrication. Each has four valence electrons, but germanium will at a given temperature have more free electrons and a higher conductivity. Silicon is by far the more widely used semiconductor for electronics, partly because it can be used at much higher temperatures than germanium. Silicon atoms form covalent bonds and can crystallize into a regular lattice. The illustration below is a simplified sketch; the actual crystal structure of silicon is a diamond lattice. This crystal is called an intrinsic semiconductor and can conduct a small amount of current. The main point here is that a silicon atom has four electrons which it can share in covalent bonds with its neighbors. These simplified diagrams do not do justice to the nature of that sharing since any one silicon atom will be influenced by more than four other silicon atoms, as may be appreciated by looking at the silicon unit cell. The electrons in the outermost shell of an atom are called valence electrons; they dictate the nature of the chemical reactions of the atom and largely determine the electrical nature of solid matter. The electrical properties of matter are pictured in the band theory of solids in terms of how much energy it takes to free a valence electron.

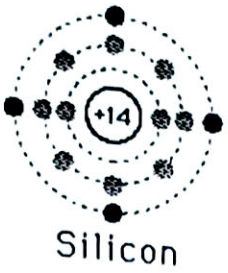
A silicon crystal is different from an insulator because at any temperature above absolute zero temperature, there is a finite probability that an electron in the lattice will be knocked loose from its position, leaving behind an electron deficiency called a "hole". If a voltage is applied, then both the electron and the hole can contribute to a small current flow. The conductivity of a semiconductor can be modeled in terms of the band theory of solids. The band model of a semiconductor suggests that at ordinary temperatures there is a finite possibility that electrons can reach the conduction band and contribute to electrical conduction. The term intrinsic here distinguishes between the properties of pure "intrinsic" silicon and the dramatically different properties of doped n-type or p-type semiconductors. Both electrons and holes contribute to current flow in an intrinsic semiconductor. The current which will flow in an intrinsic semiconductor consists of both electron and hole current. That is, the electrons which have been freed from their lattice positions into the conduction band can move through the material. In addition, other electrons can hop between lattice positions to fill the vacancies left by the freed electrons. This additional mechanism is called hole conduction because it is as if the holes are migrating across the material in the direction opposite to the free electron movement. In an intrinsic semiconductor like silicon at temperatures above absolute zero, there will be some electrons which are excited across the band gap into the conduction band and which can produce current. When the electron in pure silicon crosses the gap, it leaves behind an electron vacancy or "hole" in the regular silicon lattice. Under the influence of an external voltage, both the electron and the hole can move across the material. In an n-type semiconductor, the dopant contributes extra electrons, dramatically increasing the conductivity. In a p-type semiconductor, the dopant produces extra vacancies or holes, which likewise increase the conductivity. It is however the behavior of the p-n junction which is the key to the enormous variety of solid-state electronic devices.

The addition of a small percentage of foreign atoms in the regular crystal lattice of silicon or germanium produces dramatic changes in their electrical properties, producing n-type and p-type semiconductors. Pentavalent impurities (5 valence electrons) produce n-type semiconductors by contributing extra electrons. Trivalent impurities (3 valence electrons) produce p-type semiconductors by producing a "hole" or electron deficiency. The addition of pentavalent impurities such as antimony, arsenic or phosphorous contributes free electrons, greatly increasing the conductivity of the intrinsic semiconductor. Phosphorous may be added by diffusion of phosphine gas (PH3). The addition of trivalent impurities such as boron, aluminum or gallium to an intrinsic semiconductor creates deficiencies of valence electrons,called "holes". It is typical to use B_2H_6 diborane gas to diffuse boron into the silicon material. The application of band theory to n-type and p-type semiconductors shows that extra levels have been added by the impurities. In n-type material there are electron energy levels near the top of the band gap so that they can be easily excited into the conduction band. In p-type material, extra holes in the band gap allow excitation of valence band electrons, leaving mobile holes in the valence band.

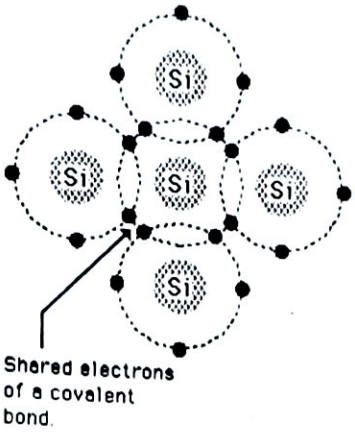
A useful way to visualize the difference between conductors, insulators and semiconductors is to plot the available energies for electrons in the materials. Instead of having discrete energies as in the case of free atoms, the available energy states form bands. Crucial to the conduction process is whether or not there are electrons in the conduction band. In insulators the electrons in the valence band are separated by a large gap from the conduction band, in conductors like metals the valence band overlaps the conduction band, and in semiconductors there is a small enough gap between the valence and conduction bands that thermal or other excitations can bridge the gap. With such a small gap, the presence of a small percentage of a doping material can increase conductivity dramatically. An important parameter in the band theory is the Fermi level, the top

of the available electron energy levels at low temperatures. The position of the Fermi level with the relation to the conduction band is a crucial factor in determining electrical properties. A useful way to visualize the difference between conductors, insulators and semiconductors is to plot the available energies for electrons in the materials. Instead of having discrete energies as in the case of free atoms, the available energy states form bands. Crucial to the conduction process is whether or not there are electrons in the conduction band. In insulators the electrons in the valence band are separated by a large gap from the conduction band, in conductors like metals the valence band overlaps the conduction band, and in semiconductors there is a small enough gap between the valence and conduction bands that thermal or other excitations can bridge the gap. With such a small gap, the presence of a small percentage of a doping material can increase conductivity dramatically. An important parameter in the band theory is the Fermi level, the top of the available electron energy levels at low temperatures. The position of the Fermi level with the relation to the conduction band is a crucial factor in determining electrical properties. For intrinsic semiconductors like silicon and germanium, the Fermi level is essentially halfway between the valence and conduction bands. Although no conduction occurs at 0 K, at higher temperatures a finite number of electrons can reach the conduction band and provide some current. In doped semiconductors, extra energy levels are added. The increase in conductivity with temperature can be modeled in terms of the Fermi function, which allows one to calculate the population of the conduction band. In terms of the band theory of solids, metals are unique as good conductors of electricity. This can be seen to be a result of their valence electrons being essentially free. In the band theory, this is depicted as an overlap of the valence band and the conduction band so that at least a fraction of the valence electrons can move through the material. In terms of the band theory of solids, metals are unique as good conductors of electricity. This can be seen to be a result of their valence electrons being essentially free. In the band theory, this is depicted as an overlap of the

valence band and the conduction band so that at least a fraction of the valence electrons can move through the material [35-36].



(a)



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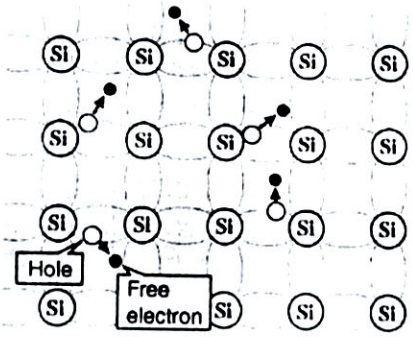


(c)

Fig. 2.1 (a) (b) Silicon crystal (c) Thermal generation of an electron-hole pair

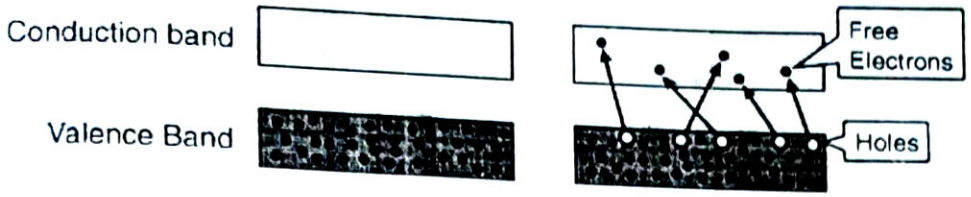


Fig. 2.2 Energy band diagram of an intrinsic semiconductor

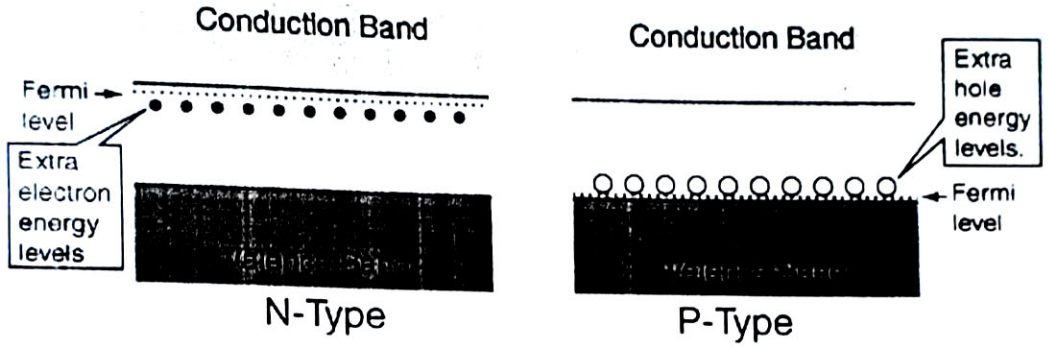


Fig. 2.3 Energy band diagram of extrinsic semiconductor showing (a) the donor level and (b) the acceptor level.

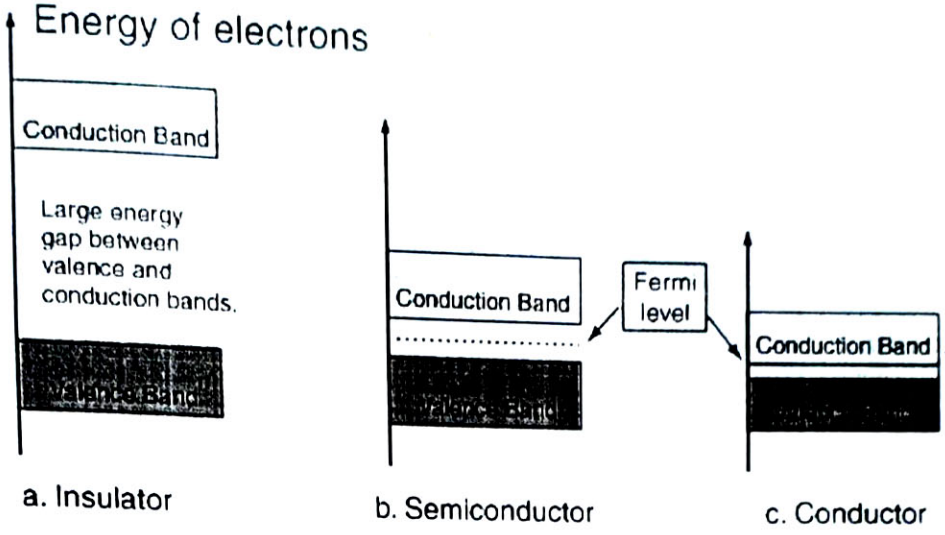


Fig. 2.4 Energy band diagrams (a) Insulator (b) Semiconductor and (c) Conductor.

2.2 Lanthanum Oxide

Lanthanum oxide (La_2O_3), also known as Lanthana is usually supplied as an odourless white powder. It is slightly soluble in water and soluble in acids [37].

Lanthanum oxide finds uses in:

- Optical glasses where it imparts improved alkali resistance
- La-Ce-Tb phosphors for fluorescent lamps
- Dielectric and conductive ceramics
- Barium titanate capacitors
- X-Ray intensifying screens
- Lanthanum metal production

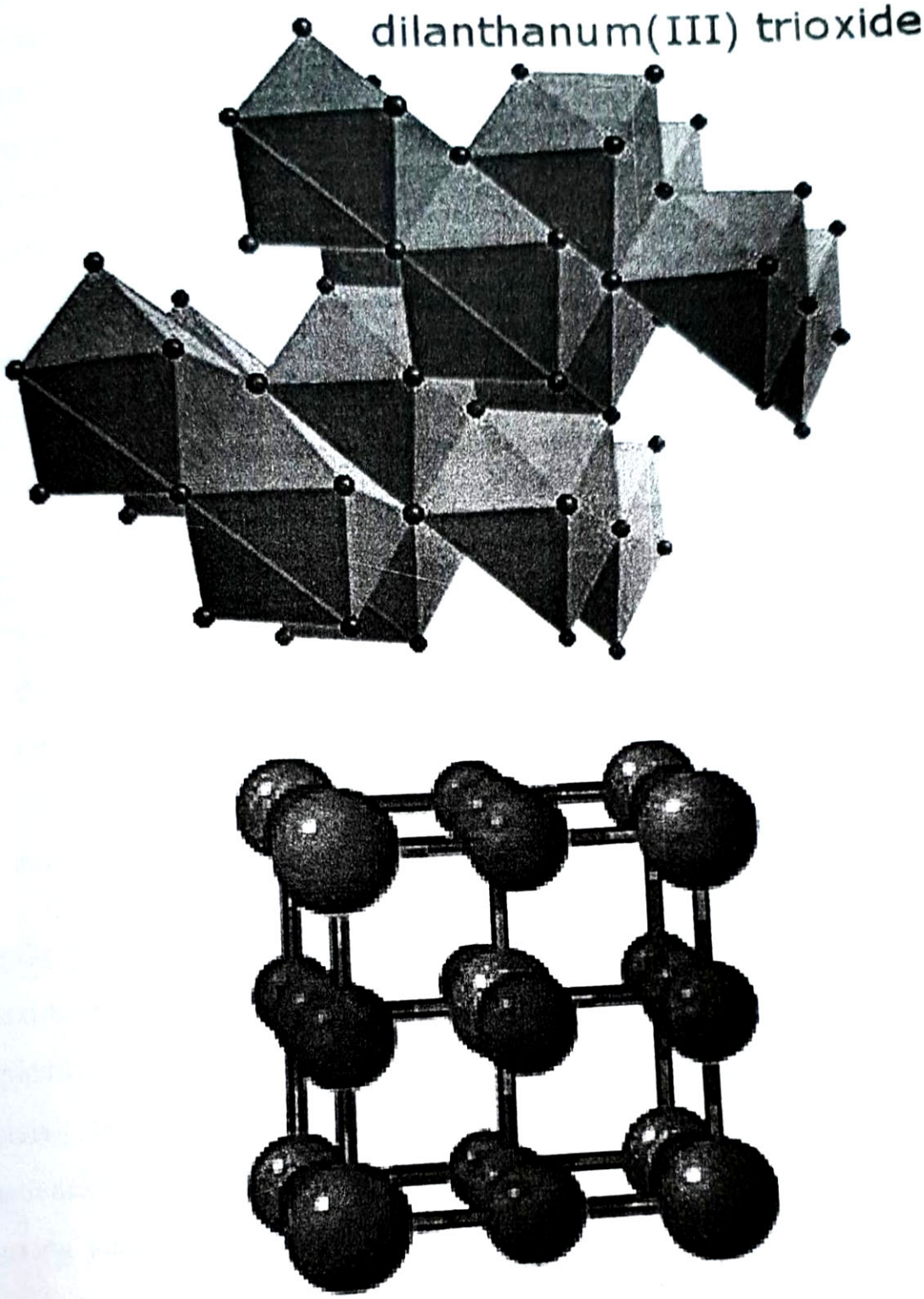


Fig. 2.5 The crystal structure of La_2O_3.

2.3 Ferrosic Oxide

Iron compounds are the most common coloring agent in ceramics. On one hand, they are nuisance impurities where they stain an otherwise white clay or glaze or where they muddy an otherwise bright color. At the same time, iron exhibits so many personalities with different kiln atmospheres, temperatures, and firing cycles and with different glaze chemistries that it is among the most exciting of all materials.

Chemically, iron is amphoteric like alumina. Fe_2O_3 generally behaves as a refractory antiflux material in a glaze melt, combining with alkalis. Oxidation iron-red glazes, for example, can have very low alumina contents yet do not run off ware because the iron acts like alumina to stabilize and stiffen the melt. However these glazes likely will have somewhat reduced durability.In glazes low in flux it can behave as an alkali, combining with silica. Fe_2O_3 is very affected by a reducing atmosphere where it can act as a flux in both bodies and glazes at high temperatures. Its fluxing action in reduction is quite remarkable and can be demonstrated using a line blend in a clear glaze. Higher amounts of iron exhibit dramatically increased fluidity.

Fe_2O_3 is the most natural state of iron oxide where it is combined with the maximum amount of oxygen. In oxidation firing it remains in this form to typically produce amber to yellow up to 4% in glazes (especially with lead and calcia), tans around 6% and browns in greater amounts. In the 20% range, matteness is typical. However, once it reduces to FeO and immediately begins fluxing and forming a glass, it is difficult to reoxidize. Since the breakdown of carbon or sulfur compounds in body and glaze so easily reduces iron, a slow and very thoroughly oxidizing atmosphere is critical through the 700-900°C range to assure that all the iron remains in its antiflux oxidized form. Most glazes will

dissolve more iron in the melt than they can incorporate in the cooled glass. Thus extra iron precipitates out during cooling to form crystals. This behavior is true both in oxidation and reduction. For example, a typical mid-temperature fluid oxidation glaze of 8-10% iron will freeze black with fine yellow crystals. Lower temperature glaze with their high flux content can dissolve more iron.

Zinc can produce unpleasant colors with iron. Titanium and rutile modify iron and can give some striking variegated effects. For example, a popular middle temperature pottery glaze employs 4% tin, iron, and rutile in a clear base to give a highly variegated gloss brown. Another popular cone 6 glaze uses 85% Albany slip, 11% lithium, and 4% tin to produce an attractive gloss brown with striations and flow lines similar to classic lead glaze effects. While many iron-stained clays are reddish in color, high iron clays can also be blackish, grey, brown and deep brown, pinkish, greenish and yellowish or maroon. Some can be quite light in color yet fire to a brown or red color. 6-7% iron is considered a high-iron clay, but some stained clay-like materials can have 20% or more iron. A typical ivory colored oxidation firing body has 1-2% iron oxide. Low temperature earthenwares can exhibit a wide range of iron red colors, depending on the firing temperature. Typically, low fired materials burn to a light orange. As temperature is increased this darkens to light red, then dark red, and finally to brown. The transition from red to brown is often very sudden, occurring across a narrow temperature range. Thus the working temperature should be sufficiently above or below this range to avoid radical color changes associated with kiln variations. Fe_3O_4 is an intermediate form of iron which is brown in color and exhibits intermediate properties. Fe_3O_4 can either be a mix of FeO and Fe_2O_3 resulting from an incomplete conversion from one type to the other, or it can be a completely different mineral form of iron known as magnetic iron oxide from the ore

magnetite. The latter is a hard crystalline material of use in producing specking in bodies and glazes [38].

Properties

Body Color - Red, Brown

In low fire the presence of iron produces red terra cotta colors that progress to brown with maturity. High temperature red bodies depend on stopping firing well short of vitrification. In higher temperature vitreous bodies fired in reduction iron is converted to actively melting black iron oxide that teams up with feldspathic melts that can dissolve benificial mullite and quartz crystals. As iron - rich liquids cool into glass, the glass has a brittle character.

Fusion – 1350°C

Glaze Color - Reddish

Low fire lead, potash and soda glazes encourage reddish colors with iron. Should be barium free.

Glaze Color - Blue

In reduction glazes Fe_2O_3 tends to fire bluish or turquoise to apple green with high soda (boric oxide may enhance). 0.5% iron with K_2O may give delicate blue to blue green.

Glaze Color - Brown

Iron produces a wide range of browns in bodies and glazes at all temperatures.

Glaze Color - Yellow

Fe_2O_3 tends to fire yellowish with calcia and in alkaline glazes straw yellow to yellow brown.In reduction, 3-4% iron with 0.4 BaO, 0.15 KNaO, 0.25 CaO, 0.2 MgO, 0.3 Al2O3, 1.7 SiO2 and 15-20% zircon opacifier will produce a yellow opaque.

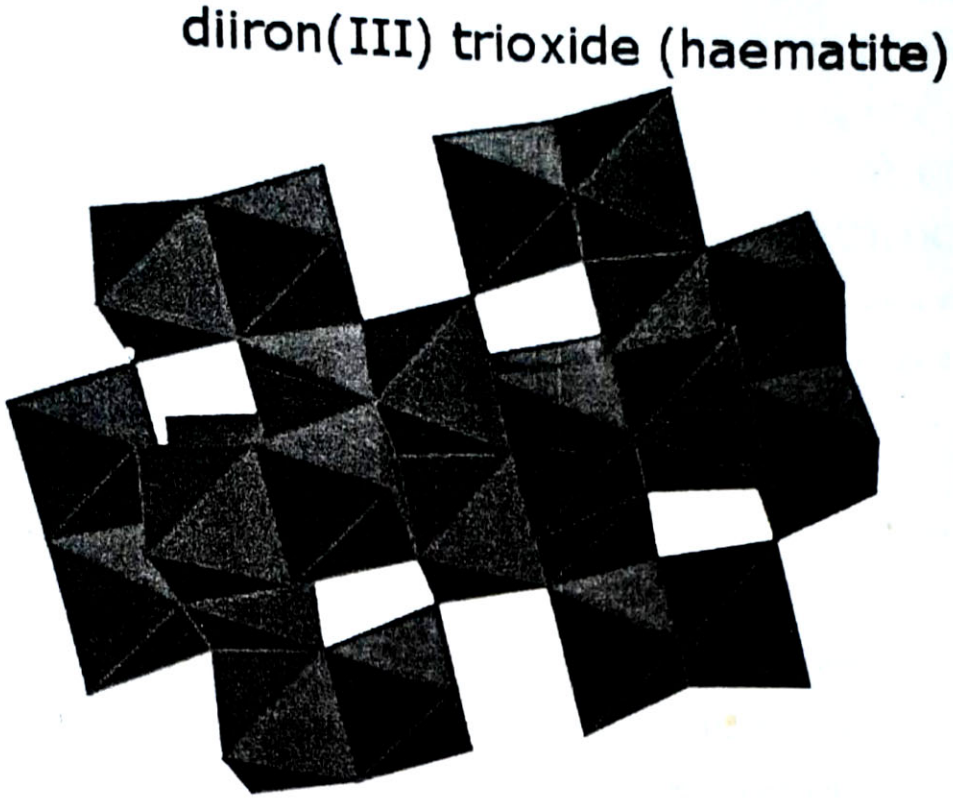


Fig. 2.6 The crystal structure of Fe_2O_3 .

CHAPTER (III)
EXPERIMENTAL PROCEDURE

3.1 Fabrication

The starting regents for (1-x) $Fe_2 O_3$ + (x) $La_2 O_3$ have been ion (III) oxide (Aldrich, purity 99.99%) and lanthanum oxide (Aldrich , purity 99.99%),. x = 0.02, 0.04, 0.06, 0.08, 0.1 were mixed by standard solid solution method . ground by agate motor, calcined at 600° C in O_2 ambient for sintering time 1hr and dried again in air. The crystalline (1-x) $Fe_2 O_3$ + (x) $La_2 O_3$, , x = 0.02, 0.04, 0.06, 0.08, 0.1 were weighed and dissolved in 2 - methoxyethanol ($CH_3 OCH_2 CH_2 OH$) solvent. The mixture solution was acidified with HCL. The solution was stirred and refluxed up to 100°C by using indirect heat treatment and cooled to room temperature, to obtain la doped $Fe_2 O_3$ precursor solution . The n- Si substrates were cleaned by standard cleaning method. The La doped $Fe_2 O_3$ precursor solution were spin - coated onto n - Si (100) substrates, to obtain films and La contents of x = 0.02, 0.04, 0.06, 0.08 , 0.1 were designed as memory devices were annealed at 600°C in air atmosphere for 1hr and cooled to room temperature. After annealing, deposited films were etched with HCL, acetone and rinsed in de- ionized water for a few minutes. Finally, the deposited film was obtained for MFS structure. Fig 3.1 depicted a schematic diagrams of our fabricated devices with MFS designs. To obtain five memory devices with various La contents ; Cu / La doped $Fe_2 O_3$ / n - Si (100), Cu electrodes (0.0314 cm^2) were contact as top electrodes and backside of the substrates were covered by Cu as bottom electrodes to be good electrical contact. The fabrication and deposition procedure was shown in flow diagram of Fig 3.2.

3.2 Ferroelectric Hysteresis Loop Measurement

The hysteresis loop is the intrinsic characteristic of ferroelectric, which is always measured with the Sawyer- Tower circuit to test ferroelectricity. A ferroelectric hysteresis loop can be observed by means of a Sawyer- Tower circuit as depicted in Fig 3.3. The external bias applied to the circuit is saw tooth wave with frequencies 100 kHz .

The optimum I (V) data were obtained from triangular voltage generators. The reason for choosing a triangular derive is that the total current I may be written as

$$I = \frac{dQ}{dt} + GV \tag{3.1}$$

Where G is the electrical conductivity and Q is the total switched charge (including polarization reversals) ; here has two terms

$$\frac{dQ}{dt} = C\frac{dv}{dt} + V\frac{dC}{dt} \tag{3.2}$$

Fig 3.4 shows the ferroelectric hysteresis loop. If we first apply a small electric field, we will have only a linear relationship between P and E because the field is not large enough to switch any domain and the crystal will behave as a normal dielectric material.

A ferroelectric capacitor has a highly nonliear dielectric with permanent charge retention after application of a voltage by an external circuit. The permanent charge originates from a net ionic displacement in unit cells of the compensating charge to flow onto the capacitor plates. If the field is applied in material resulting from the external voltage application. The individual unit cells interact constructively with their neighbours to produce domains within the material. As the voltage is removed the majority of the domains will remain poled in the direction of the electric field, required compensating charge causes a hysteresis in the standard charge vs voltage plot of the capacitor as it is cycled through positive

and negative voltage application. Using the Sawyer-Tower circuit, P-E characteristic and remanent polarization versus bias voltage are studied.

3.3 Capacitance Versus Voltage Characteristics Measurement

The space-charge region in a p-n junction consists of a dipole layer of charges produced by donor and acceptor ions. In the depletion approximation, the magnitude of the space charge per unit area Q_d on either side of the junction can be written as

$$Q_d = qN_a \mid x_p \mid = qN_d \mid x_n \mid \tag{3.3}$$

Since x_n and x_p are functions of the junction voltage, Q_d varies with the voltage. A change in the bias voltage causes readjustment of x_n and x_p to their appropriate new values. This change is accomplished by the movement of majority carriers in or out of the space – charge layer. The situation is similar to the charging and discharging of a parallel plate capacitor. However, the junction space-charge layer capacitance differs from an ordinary parallel plate capacitor in one important respect. In the parallel plate capacitor the charges reside on the two plates, and the capacitance is independent of voltage. In the depletion layer, the charges are distributed in a region of space whose thickness increases nonlinearly with the voltage. Therefore, the charge Q_d also varies with the voltage in a nonlinear manner. Because of its nonlinear behavior, the junction capacitance C_j can be defined for only small change dV_a in the junction voltage

$$C_j = A\frac{dQ_d}{dV_a} \tag{3.4}$$

Substitution for Q_d from eqn. (3.3),

$$C_j = qA\left(\frac{N_d N_a}{N_d + N_a}\right)\frac{dW}{dV_a} \tag{3.5}$$

Finally,

$$C_j = A\left(\frac{q\varepsilon_s}{2(V_i - V_a)} N_I\right)^{1/2} \tag{3.6}$$

where $N_I = (N_d N_a)/ (N_d+N_a)$ represents the effective dopant concentration. There are two useful ways in which equation (3.6) can be rewritten.

$$C_j = \frac{C_o}{\left(1 - \frac{V_a}{V_i}\right)^{1/2}} \tag{3.7}$$

where C_o is the zero-bias capacitance.

$$C_j = \frac{\varepsilon_s A}{W} \tag{3.8}$$

This relation shows that the junction capacitance can be regarded as the capacitance of a parallel plate capacitor with separation between the plates as the depletion region width W.

The relation in equation (3.8) further shows that for a given bias, the capacitance C_j can be uniquely defined only for small changes in the junction voltage that cause a negligible change in W. Fig (3.5) is the junction has a depletion region with W at the bias voltage V_a. When the voltage is changed between $V_a+\Delta V_a$ and $V_a-\Delta V_a$, the depletion region width varies between $W-\Delta W$ and $W+\Delta W$. As long as ΔW is small compare to W, the capacitance C_j is given by equation (3.8). If ΔV_a is large enough to make ΔW comparable to W, then equation (3.8) does not given the proper value of C_j.

From equation (3.6) it is seen that C_j varies inversely with the square root of $(V_i - V_a)$. Since this relation is based on the depletion approximation, it is valid under reverse bias. It may also be valid under a small forward bias if V_i is of the order of 1V.

Measurement of C_j as a function of reverse bias can be used to determine the built-in voltage V_i and the a dopant concentration near the junction.

According to equation (3.6) a plot of $C_j^{-1/2}$ as a function of V_a is a straight line whose intercept on the voltage axis gives V_i, and the slope can be used to determine the effective dopant concentration [39]. In order to show the electrical properties of the ferroelectric capacitor, the capacitance of the sample are measured using the LCR Digibridge Quad Tech Meter (Model-1730).

3.4 Current Versus Voltage Characteristics Measurement

When a voltage is applied to a p-n junction diode, the electron and hole distributions in the space - charge and neutral regions are changed from their equilibrium values. The diode current is intimately related to these distributions. To be specific, Let us consider the forward - biased diode Fig 3.6 (a) . The hole and electron distributions in various regions of the diode are shown in Fig 3.6 (b). The applied bias causes the majority carriers in the neutral n - and p - regions is increased. To maintain the space- charge neutrality in these regions, the majority carrier concentrations also increase by the same amount. These changes, however, are not visible in the plots of Fig 3.6 (b) because , under the level of injection considered here, the charges in the majority concentrations are negligibly small compared to their thermal equilibrium values.

It is not necessary to specify the exact form of the electron - hole distributions at this stage. However, if we confine our attention to holes in the n region, it becomes clear that an increase in the hole concentration at the edge x_n causes a flux of holes toward the contact at w_1. As these holes move away from x_n, they recombine with electrons and their concentration decreases gradually, reaching an equilibrium value at a few diffusion lengths away from x_n. Accordingly , in the neutral n- region the hole current has its maximum value at x_n and decreases continuously to become zero at large distances. Similarly, in the neutral p - region , the electron current has its maximum value at $-x_p$ and decreases away

from it . Since the electron - hole currents are functions of position, a reference point is needed at which they can be easily evaluated. The edges of the space - charge layer x_n and $- x_p$ are two such reference points. The hole and electron currents evaluated at these points are added together to obtain the total diode current.

At low - level injection,

$$P_n(x_n) = P_{no} \exp(Va / V_T) \qquad (3.9)$$

where $P_n(x_n)$ = the hole concentration

V_a = the applied voltage to the diode

V_T = the thermal voltage

The ideal diode current voltage characteristics is described by equations

$$I = I_s \left[\exp(V_a/V_T) - 1\right] \qquad (3.10)$$

$$I_s = qAn_i^2\left(\frac{D_P}{N_d L_P} + \frac{D_n}{N_a L_n}\right) \qquad (3.11)$$

Where ,

I_s = reverse saturation current

N_d = the total donor concentration

D_n, D_p = Diffusion coefficient

N_a = the total acceptor concentration

L_p , L_n = electron and hole diffusion length

A = the junction area

n_i = the intrinsic electron concentration

It is seen that in the forward direction, the current I rises exponentially with the voltage, whereas in the reverse direction, it saturates to a value I_s . These features are evident from Fig 3.6 (c).

Our discussion until now has been confined to an abrupt p-n junction. In a linear graded junction, the calculation of diode current is complicated by the fact that, because of concentration gradients, an electric field is also present in the neutral n- and p- regions. This field is in a direction so as to retard the flow of injected minority carriers. However, it does not have any masked influence on the form of the I-V characteristic. When the grading constant K is sufficiently large to produce a well - defined space- charge region at the junction , the Boltz- mann boundary condition equation (3.9) is still satisfied. Thus, we obtain the ideal diode equation for the linearly graded and other types of junctions independent of the impurity distribution [40].

It is often convenient to add the diffusion and the depletion region generation recombination currents together in a single expression by writing the equation as

$$I = I_o [\exp (V_a / \eta V_T) - 1] \qquad (3.12)$$

Where,

$I_o = I_s$ when the diode current is dominated by the diffusion process, and $I = I_{RO}$ when the current is dominated by the depletion region generation - recombination process. The parameter η, known as the ideality factor , has a value of 1 for the diffusion current and is approximately 2 for the recombination current . When the two currents are comparable, η lies between 1 and 2. The current I_o can be determined experimentally by extrapolation the forward log I versus V_F plot to zero bias. I -V characteristics can be measured by a FLUKE SCOPE METER (model - 196). In this study, an effort was made to observe the current- voltage behavior of the device, to not only provide guidelines for using them of device characterization but also establish an improved decision to account for electrical behavior of schottky - like ferroelectric memory diode [41].

3.5 Transient Current Versus Time Characteristics Measurement

The temperature dependence of the transient current characteristic in the ferroelectric thin film capacitors have been studied by I-t measurement in the temperature 600°C. The I-t characteristics are measured at various frequencies using the simple C-R circuit as a differentiator with a FLUKE SCOPE METER (Model – 196) as illustrated in fig. 3.7 (a ~ c). At applied voltage range from 2V to 10V, the transient current of La doped Fe_2O_3 are measured at frequency range from 1kHz to 100kHz.

The transient current consists of two components, the electric conduction current and the polarization current. The trapped holes causes and increase of the local electric field and hence the conduction current. The transient current at low stress voltage is mostly clue to the polarization current. When the spontaneous polarization reverse a displacement current to flow in the resistor. The current clue to reversal of the polarization is called the switching current or the transient current. The transient current for charging and discharging are determined by measuring the voltage drops through the resistor. Depending on the relative magnitude of the current components, the transient current characteristics can be separated into two different type, the degradation type and polarization type [42-43].

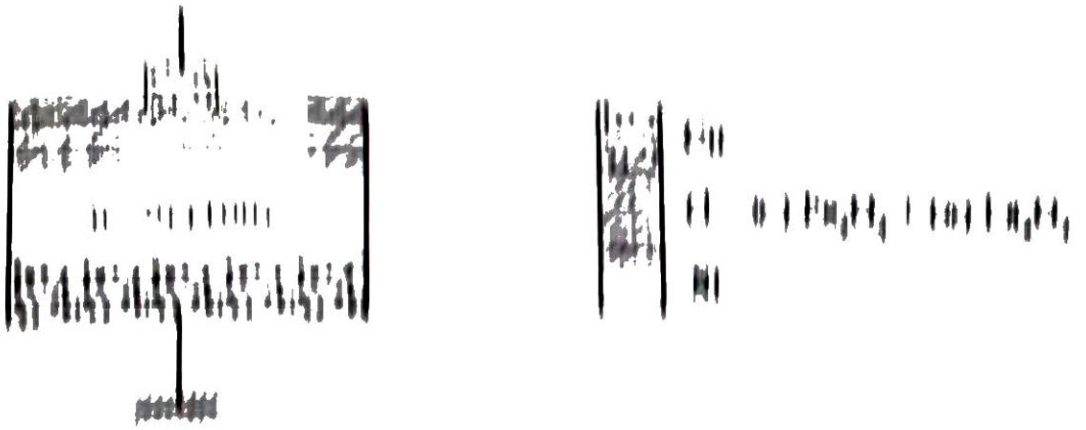


Fig. 1.1 [illegible]

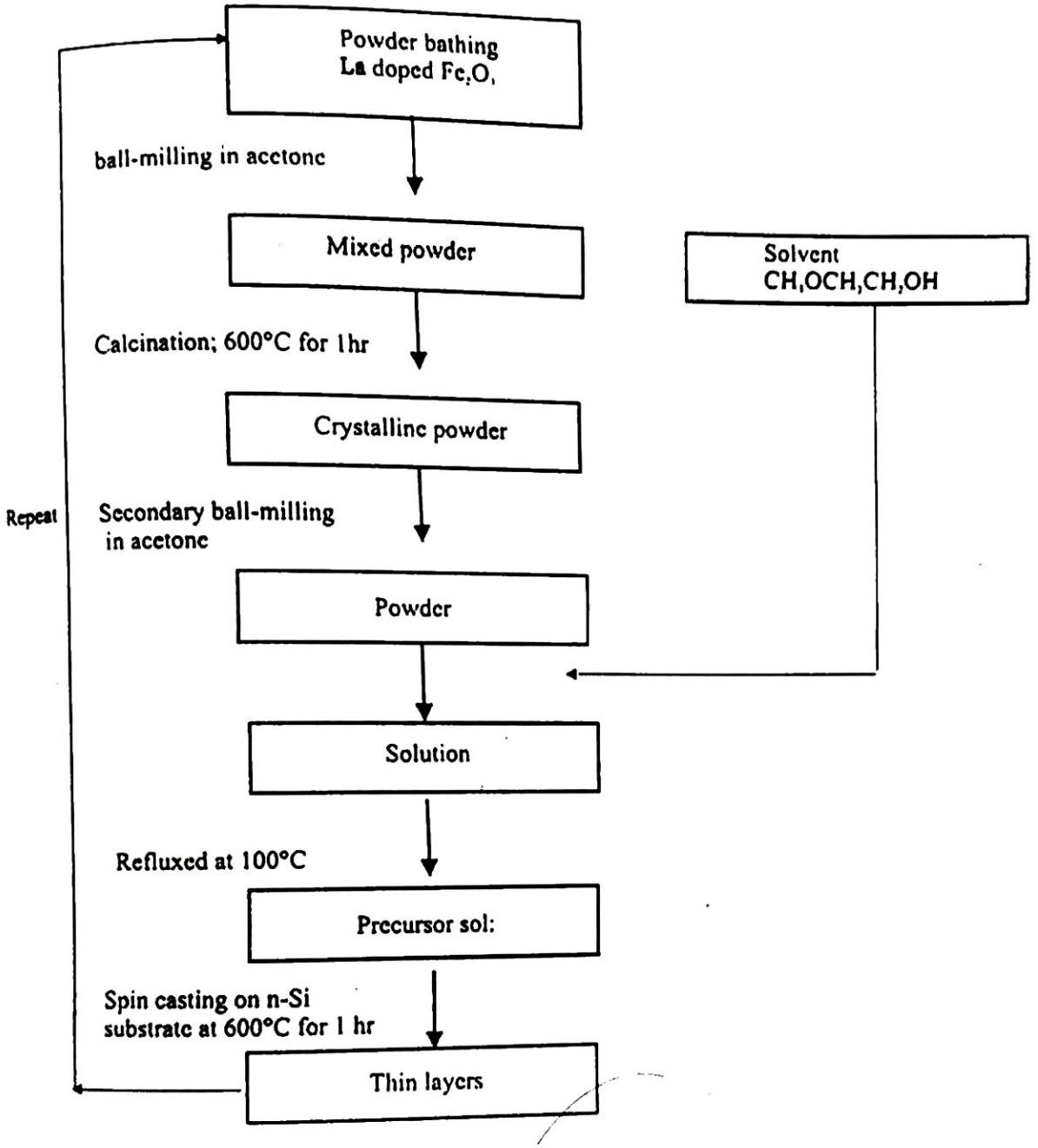


Fig 3.2 Flow diagram for fabrication of (1 -x) Fe_2O_3 + (x)La_2O_3 thin layers.

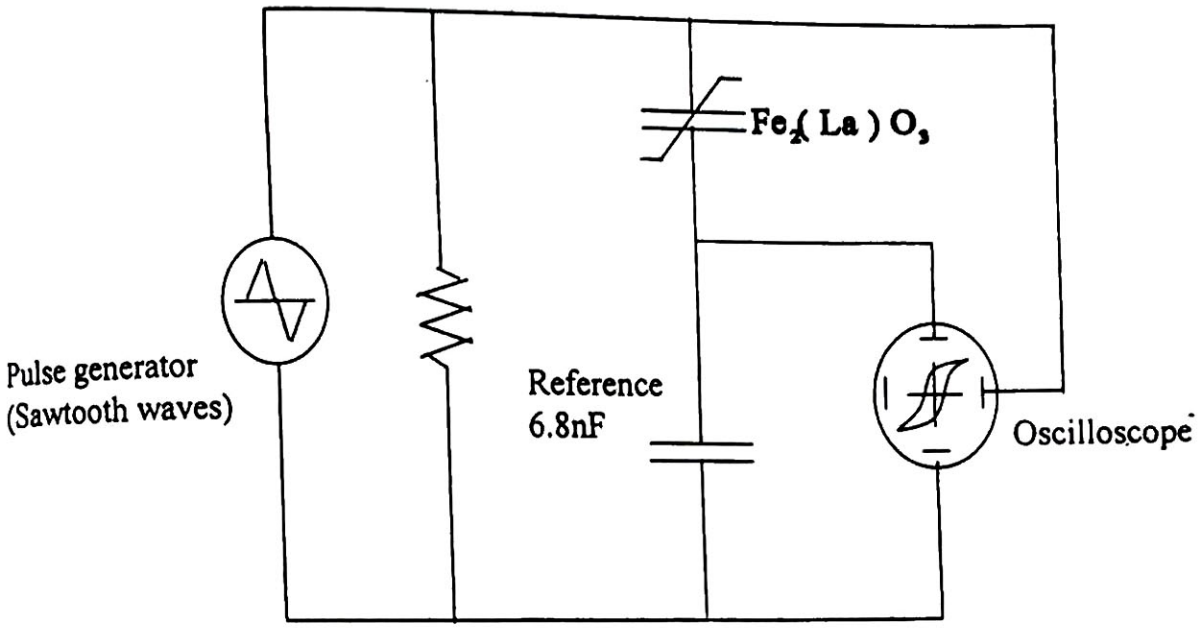


Fig 3.3 Measurement of Polarization with Sawyer - Tower Circuit.

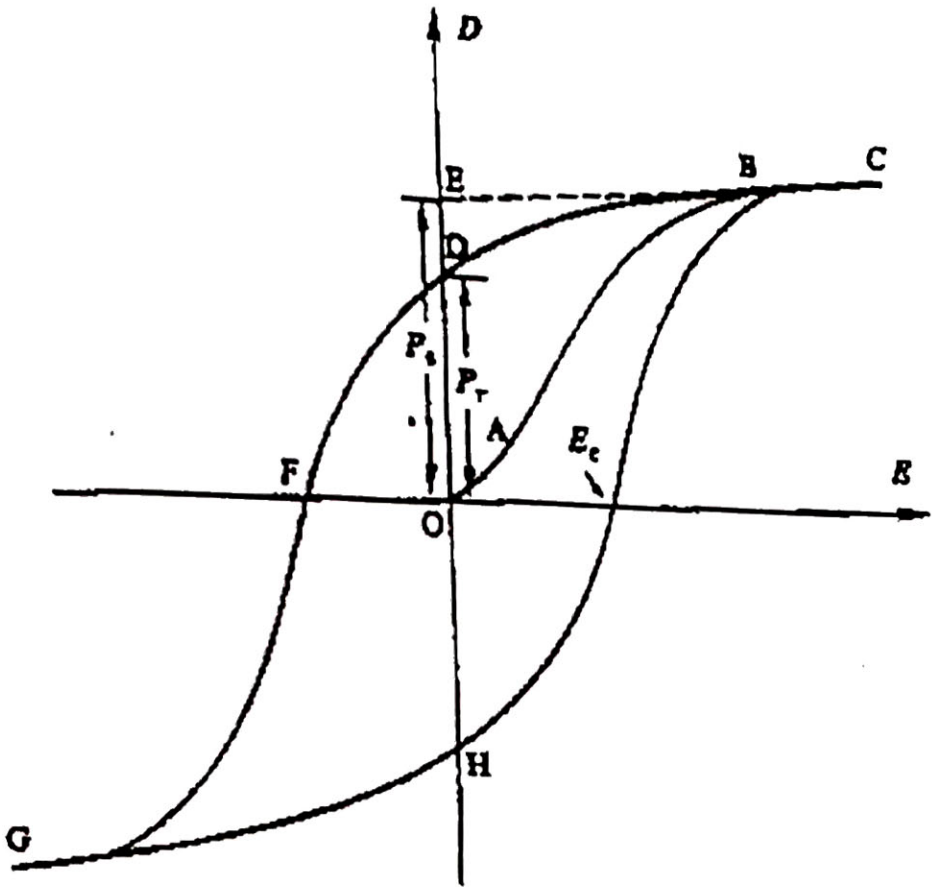


Fig 3.4 A Typical P-E Hysteresis Loop observed with Ferroelectric sample.

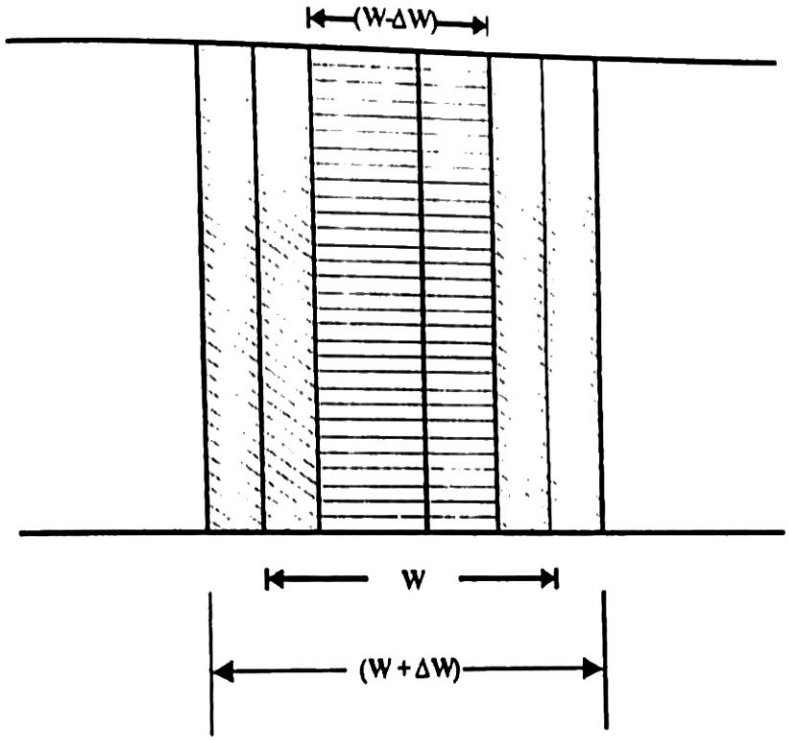
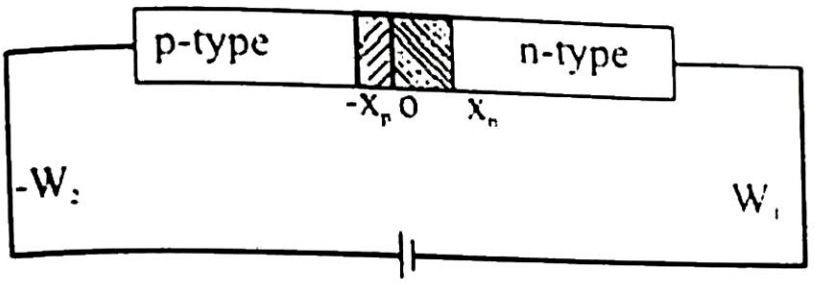
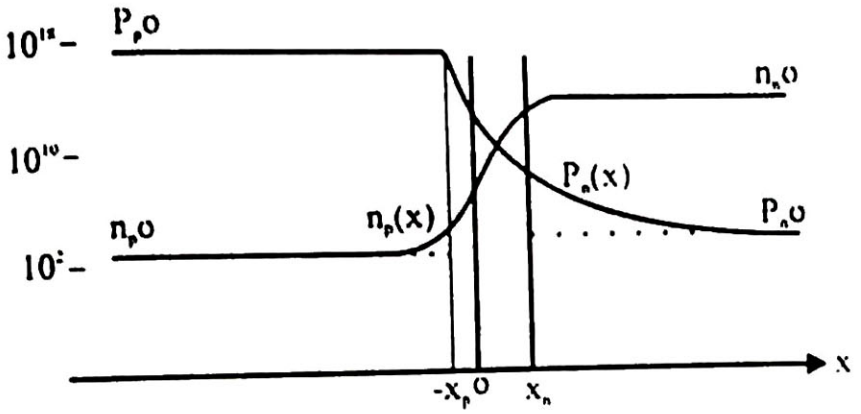


Fig 3.5 Change in the depletion region width caused by an increment ΔV_a in the junction bias.



(a)



(b)

Fig 3.6 (a) Schematic diagram of a forward - biased p-n junction diode and

(b) Electron- hole distributions in the various regions.

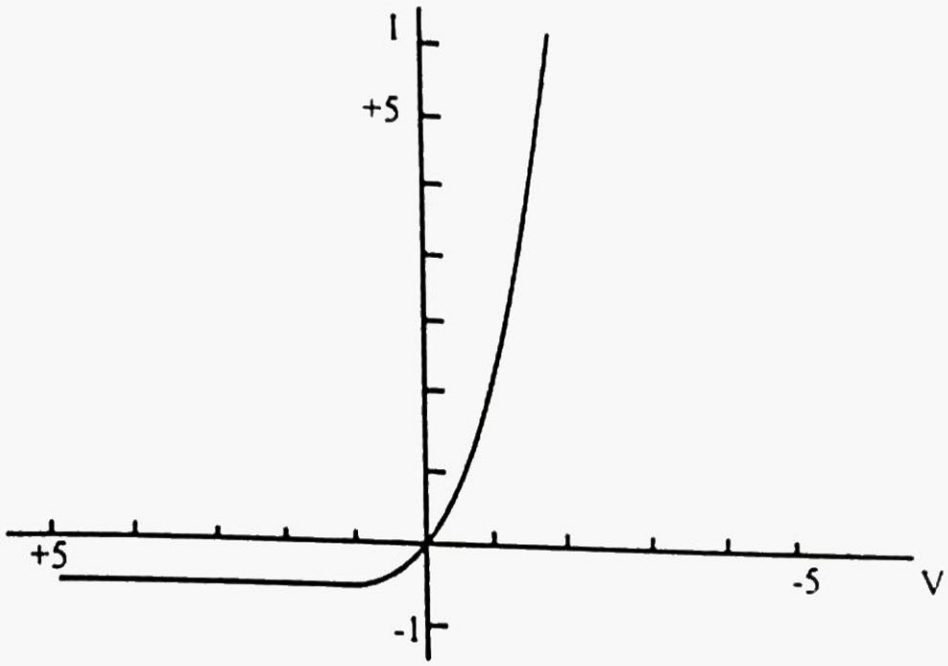
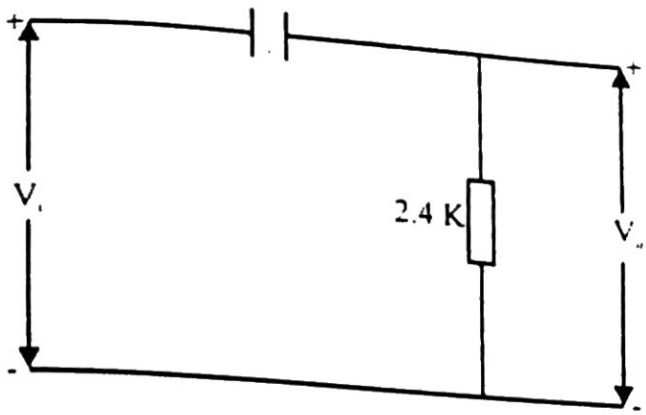
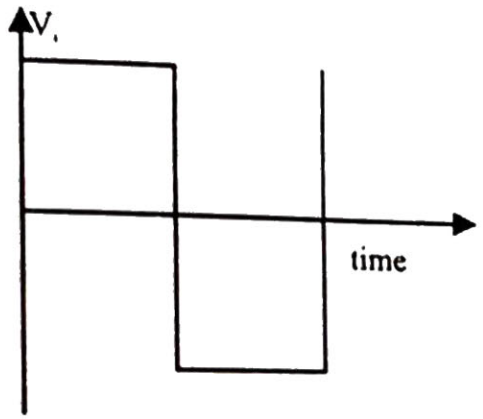


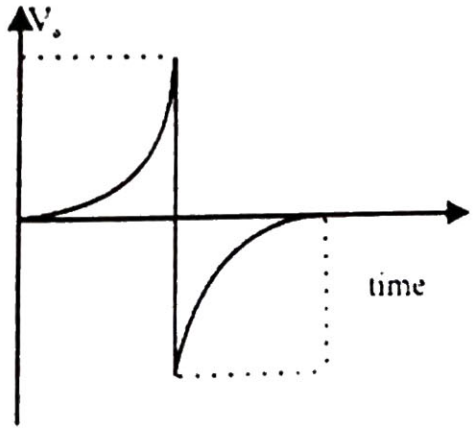
Fig 3.6 (c) Ideal diode current-voltage characteristic.



(a)



(b)



(c)

Fig 3.7 (a) Simple C-R circuit

(b) Square Wave Input

(c) Pulse Response of Simple C-R circuit

CHAPTER IV
RESULTS AND DISCUSSION

4.1 Ferroelectric Characteristics

Fig. 4.1 (a ~ e) depict the P-E characteris of La doped Fe_2O_3 (dopant La composition x = 0.02, 0.04, 0.06., 0.08 and 0.10 respectively) thin film devices heat treated at 600°C. From the characteristics, the remenant polarization P_r, the spontaneous polarization P_s, coercive field E_c and memory window MW can be measured. It is examined that hysteresis loops are symmetric and it may be due to polarization or space charge. Fig. 4.2 indicates the variation of bias voltage (V_{pp}) with remanent polarization ($2P_r$) of the thin film devices. It is observed that remanent polarization increases while bias voltage is raised. Fig. 4.3 shows the dependence of La composition on coercive field of the thin film devices at V_{pp} = 10V. It is examined that coercive field increases with increasing La composition to Fe_2O_3 thin film devices. Fig. 4.4 indicates the variation of spontaneous polarization with La composition to thin film devices. It is obvious that spontaneous polarization gradually increases with La composition to thin film devices. Fig. 4.5 represents the dependence of memory window with La composition to thin film devices. The width of the memory window is very important to fabricate the memory devices. It is obvious that the width of the memory window also increase with La composition to Fe_2O_3 thin film devices.

4.2 Capacitance – Voltage Characteristics

Memory effect of C-V curves are measured to study whether the ferroelectric films can control the Si surface. Fig. 4.6 (a ~ e) show the 100 kHz C-V characteristics of Cu/La doped Fe_2O_3 / n-Si (100) composition x = 0.02, 0.04,

0.06, 0.08 and 0.10 respectively. The counterclockwise C-V hysteresis indicated by the arrows shows that the capacitance changes from the accumulation to inversion states and that the memory windows of the hysteresis under the bias condition. The counterclockwise hysteresis means that ferroelectric hysteresis controls the Si surface potential and suggested this could be applied to MFS-FET type memory device. Variation of dopant concentration with threshold voltage of La doped Fe_2O_3 thin films are indicated in Fig. 4.7. Composition dependence of flat band voltage (up and down) of La doped Fe_2O_3 thin films are depicted in Fig. 4.8. Composition dependence of the memory window of the La doped Fe_2O_3 thin films is indicated in Fig. 4.9. It is obvious that the width memory window gradually increases with increasing La composition. Some parameters derived from C-V variations are threshold voltage (swept up and swept down), flat-band voltage (swept up and swept down), the width of memory window which are collected in Table 4.1.

Table (4.1) Memory width, threshold voltage and flat-band voltage of La doped Fe_2O_3 thin film capacitors with Cu electrode.

La composition	Memory width (V)	Threshold voltage (V)		Flat-band Voltage (V)	
		Up	Down	Up	Down
x = 0.02	0.9722	1.6667	1.1111	9.1667	8.3333
x = 0.04	1.3889	- 5.2778	- 6.3889	1.3889	0.5556
x = 0.06	1.5556	2.2222	1.1111	7.2222	8.8889
x = 0.08	1.9444	- 3.3333	- 4.7222	2.2222	0.8333
x = 0.10	1.6667	- 1.9444	- 3.8889	2.7777	1.1111

4.3 Current – Voltage Characteristics

I-V characteristics are measured with a digital scope meter (FLUKE, 196) to evaluate the magnitude of the leakage current density in the film. The voltage applied to the copper electrode is positive for the n-type Si substrate, that is the measurements are performed in the accumulation region in n-Si substrates. I-V characteristics are obtained at room temperature for La doped Fe_2O_3 thin film device heat treated at 600°C for 1 hr, and are shown in Fig. 4.10 (a ~ e). The Schottky diodes have been made on a number of semiconductors, and most of the devices follow the I-V relation of the form

$$I = I_S \exp \frac{V}{\eta V_T} \qquad (4.1)$$

where is called the ideality factor, I_S is the forward saturation current V_T is, the threshold voltage, 0.02586 V for room temperature and V is the bias voltage drop across the semiconductor surface depletion layer. For an ideal Schottky diode, $\eta = 2$. Factor that make to exceed unity are: (1) the bias dependence of barrier height, (2) the tunneling of electrons through the barrier, and (3) the electron-hole pair recombination in the depletion region. In these measurements the diode current I is measured as a function of the forward bias and ln I is plotted against the bias voltage. The saturation current, I_S, is obtained by extrapolation the straight line to V = 0. If the diode are A and the Richardson constant R* are known, zero bias barrier height ϕ_{bo} can be obtained from equation (4.2).

$$I_S = AR^* T^2 \exp\left(-\frac{q\varphi_{bo}}{KT}\right) \qquad (4.2)$$

where $R^* = 4\pi m_e q k^2/h^3$, R* for the thermonic emission of electron from the metal into the semiconductor having electron effective mass m_e, R* is 8.16 AK^{-2} cm^{-2} at room temperature.

The Schottky I-V characteristics at 300 K are shown in Fig. 4.10 (a ~ e) for all samples. Fig. 4.11 (a ~ e) represent the forward semi-log I-V characteristics of Schottky-like diodes grown on n-Si (100) with all La doped Fe_2O_3 thin films of MFS designs. These plots clearly depict the linearity. The gradually shift of the I-V plots towards a higher voltage is observed. In the film on the Si substrate the current density-voltage curve is slightly asymmetric which might indicate the barrier-limited Schottky emission due to the asymmetric structure of the copper electrodes. Using equation (4.1) the value of the ideality factor of the device at various La doped Fe_2O_3 thin film devices are calculated from the slopes of the linear regions of the semilog forward bias curve. Using equation (4.2), the zero-bias barrier height, ϕ_{bo}, is determined from the extrapolated experimental saturation current, I_S. Zero-bias barrier heights from I-V measurement also increase with increasing dopant content. The zero-bias barrier height versus compositions is shown in Fig. 4.12. The ideality factor versus composition is shown in Fig 4.13. The diode ideality factors (η) and zero-bias barrier height (ϕ_{bo}) are examined by equations (4.1) and (4.2) and the evaluated values are listed in Table 4.2.

Table 4.2 **Electrical parameters derived from the analysis of I-V characteristics and the value of I and V = 5V.**

Parameter / Sample with La doped	Ideality factor η	Zero-bias barrier height ϕ_{bo} (eV)	I (mA) at V = 5V
Sample 1 x = 0.02	0.87	0.34	7
Sample 2 x = 0.04	0.78	0.36	8
Sample 3 x = 0.06	1.53	0.23	8.5
Sample 4 x = 0.08	1.55	0.41	8
Sample 5 x = 0.10	1.56	0.40	10

4.4 Switching Transient Characteristics

The transient current for charging and discharging are determined by measuring the voltage drops through a 20kΩ resistor being connected with La doped Fe_2O_3 thin films with copper electrode by own sol-based method are studied. The polarity is defined to be positive when a positive voltage is applied to the top electrodes. The La composition effect of transient current is determined at process temperature 600°C Fig. 4.14 (a ~ e) indicate the I-t characteristics of Cu/La doped Fe_2O_3 / n-Si (100) thin films at process temperature 600°C. It is found that transient current of La doped Fe_2O_3 at process temperature of 600°C for 1 hr in O_2 – ambient is conduction current type in the applied voltage range from 2V to

10V. From these figure, it is clearly obvious that the transient current slowly increases with time for all thin films with copper electrode and it may be due to the enhancement of the local electric field caused by the accumulation of trapped holes. It is also known that the degradation–type of transient current is formed.

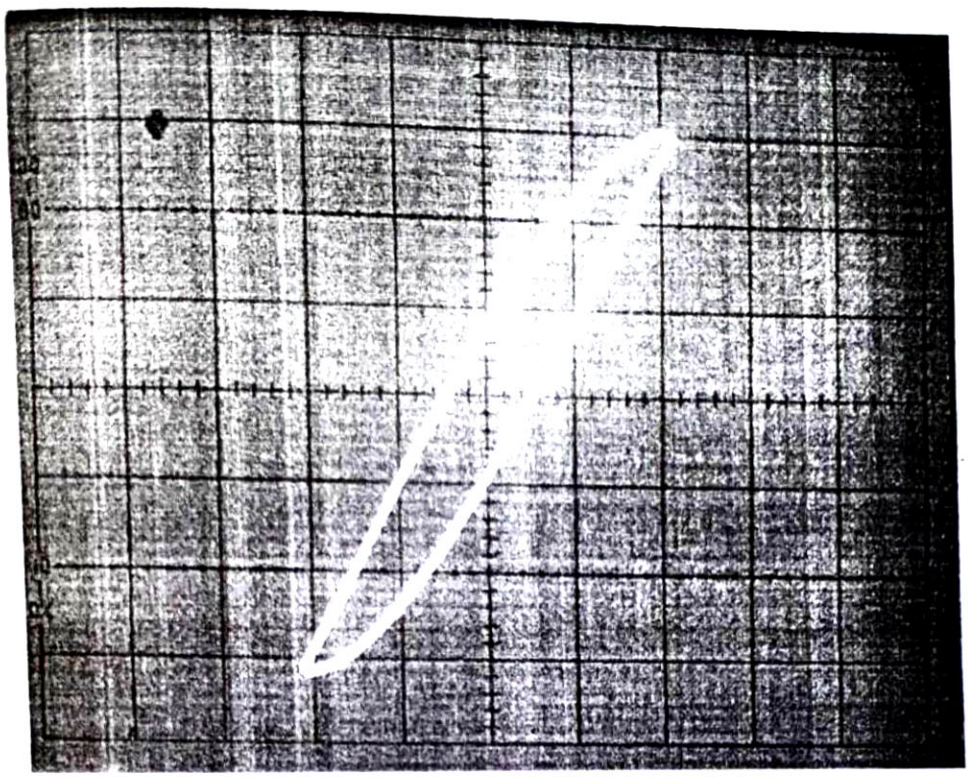
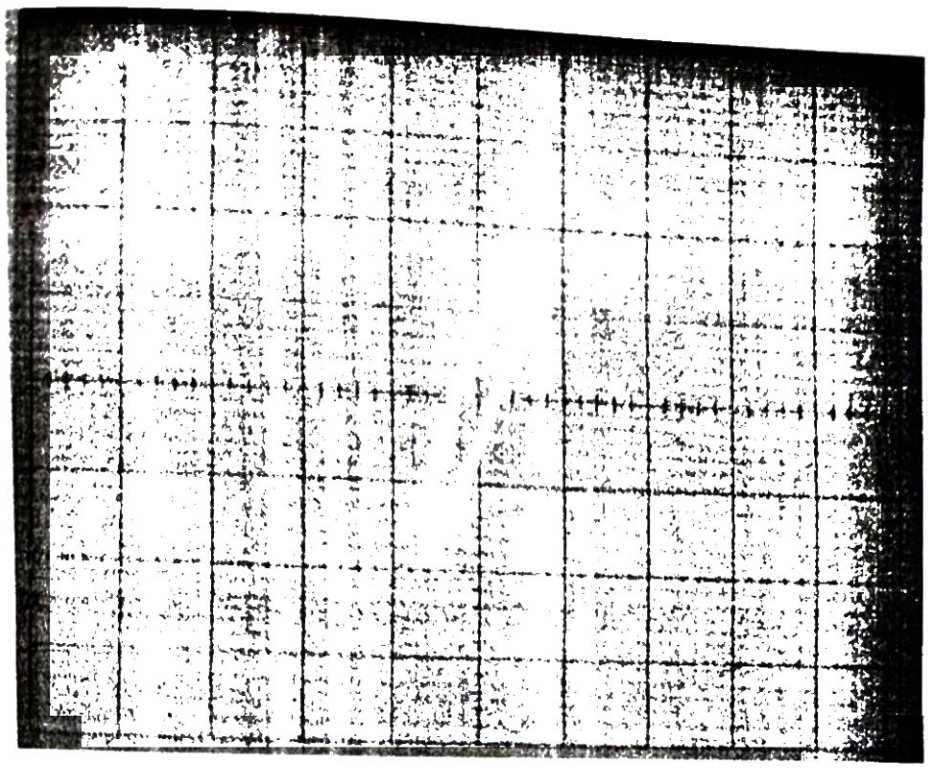


Fig. 4.1(a) P-E hysteresis loop of La doped Fe_2O_3 (x = 0.02) thin film capacitor (formed at 600°C) with Cu electrode.



4.1(b) P-E hysteresis loop of La doped Fe_2O_3 (x = 0.04) thin film capacitor (formed at 600°C) with Cu electrode.

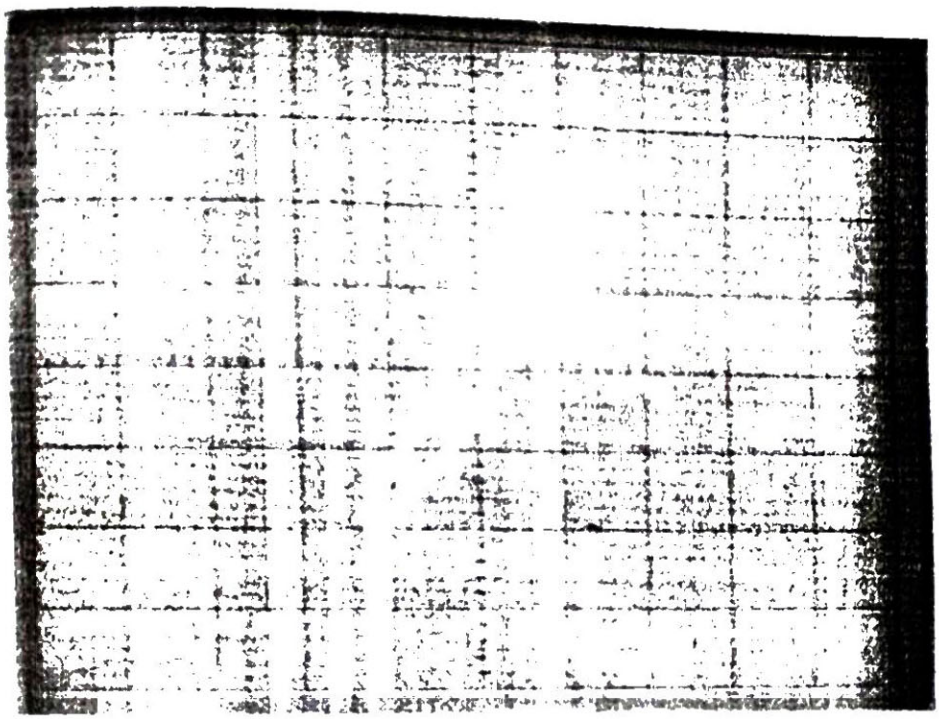


Fig. 4.1(c) P-E hysteresis loop of La doped Fe_2O_3 (x = 0.06) thin film capacitor (formed at 600°C) with Cu electrode.

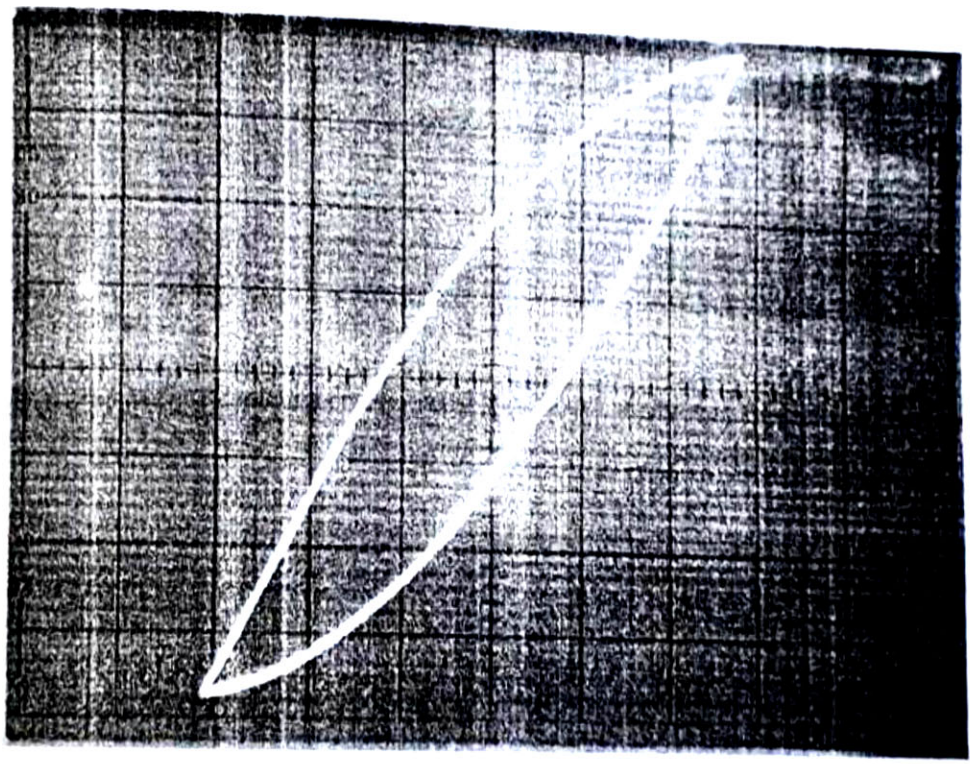


Fig. 4.1(d) P-E hysteresis loop of La doped Fe_2O_3 (x = 0.08) thin film capacitor (formed at 600°C) with Cu electrode.

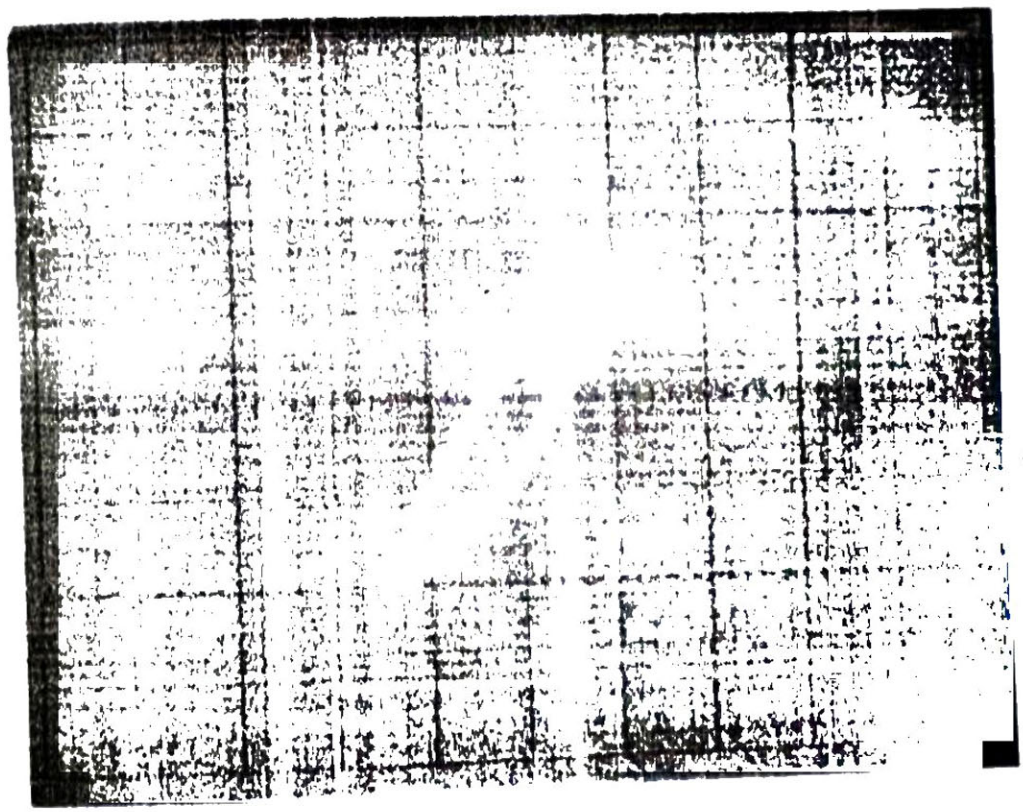


Fig.4.1(e) P-E hysteresis loop of La doped Fe_2O_3 (x = 0.10) thin film capacitor (formed at 600°C) with Cu electrode.

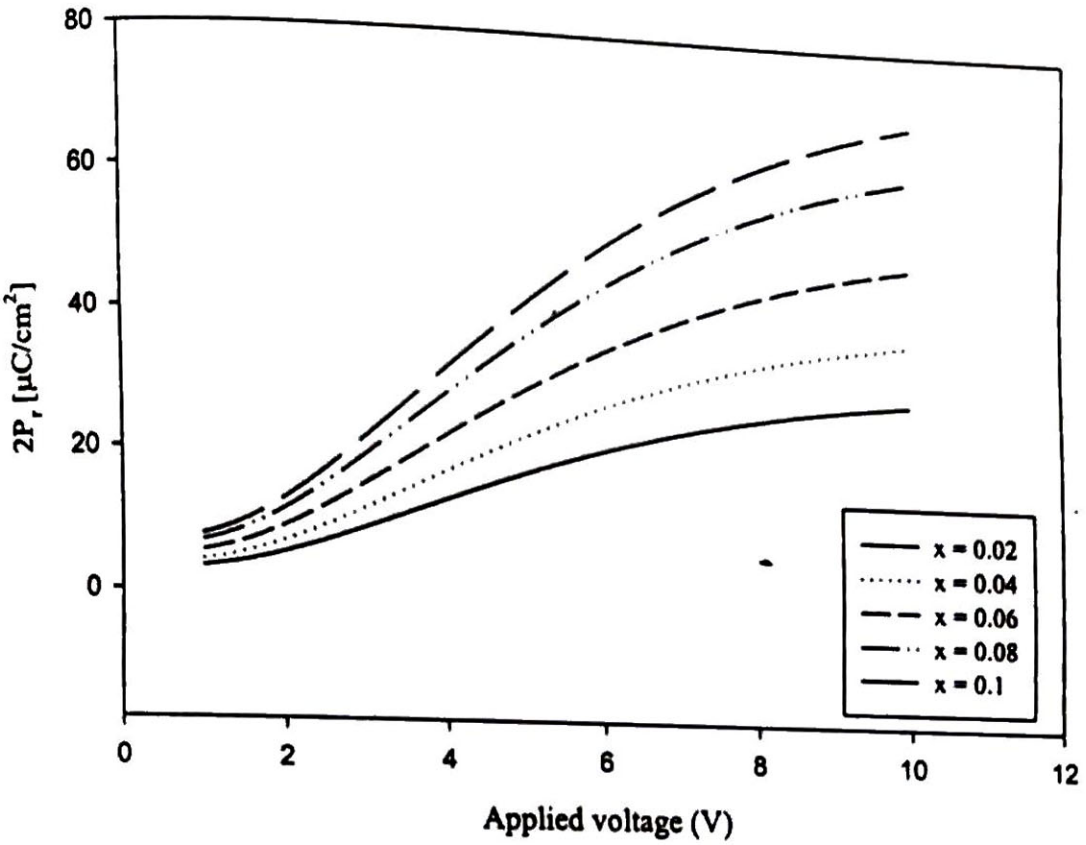


Fig.4.2 Saturation properties of remanent polarization of La doped Fe_2O_3 thin films device with Cu electrode.

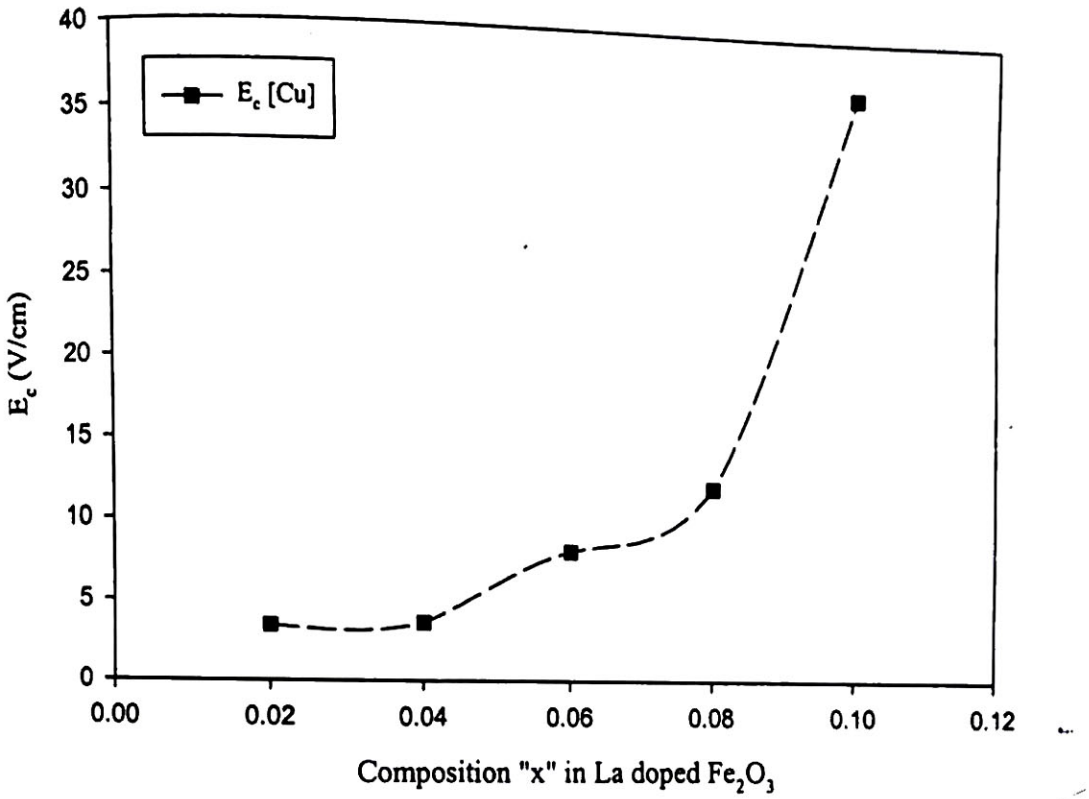


Fig.4.3 Composition dependence of the coercive field of La doped Fe_2O_3 thin film device.

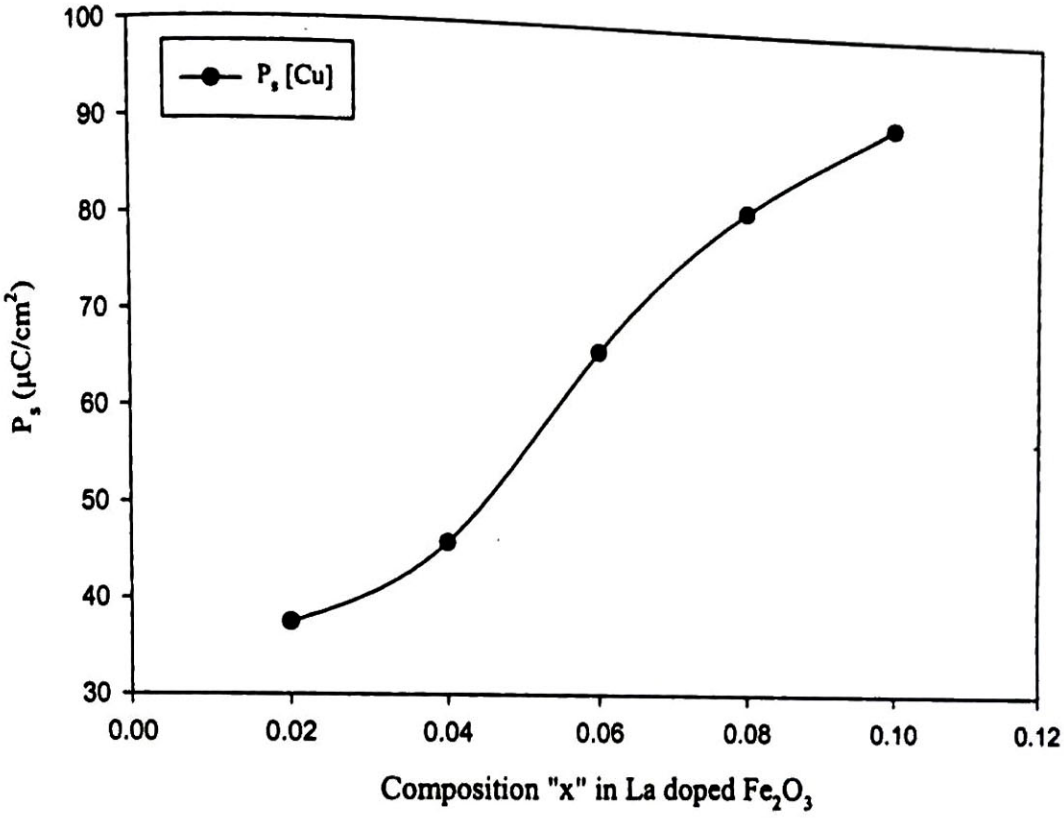


Fig.4.4 Composition dependence of the spontaneous polarization of La doped Fe_2O_3 thin film device.

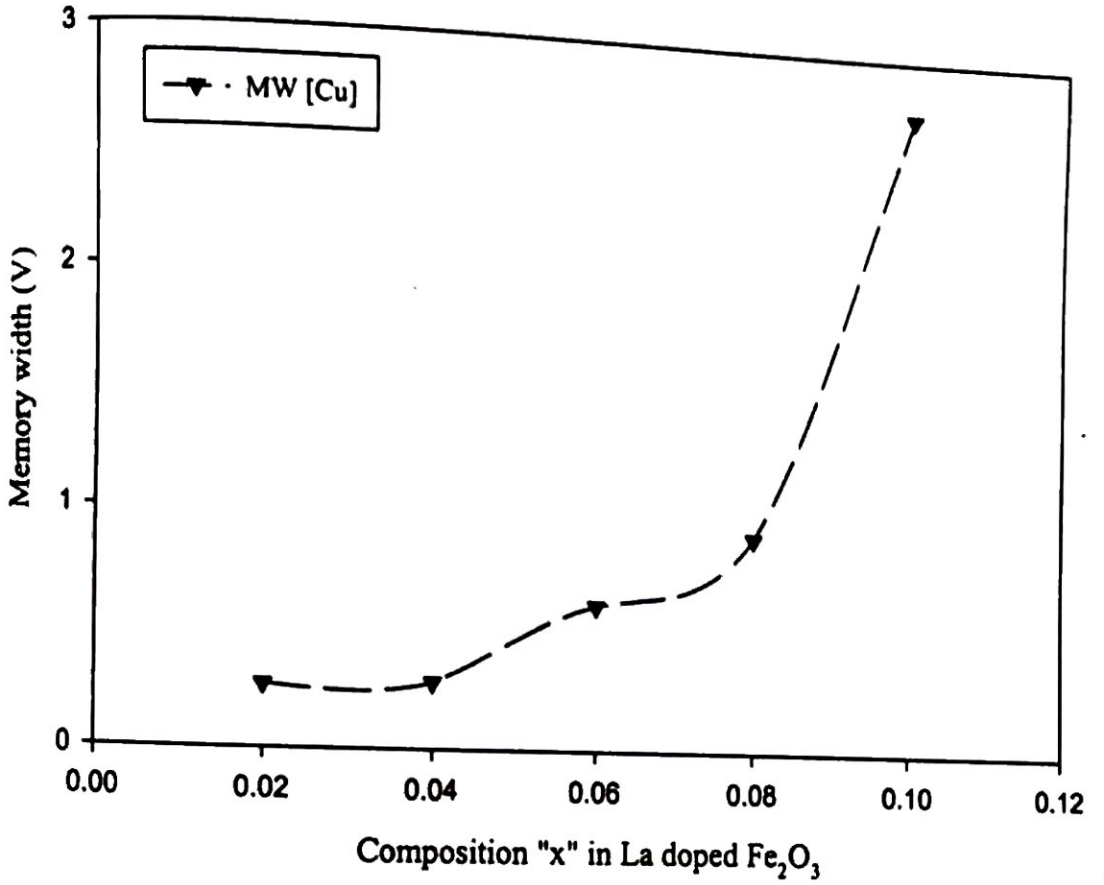


Fig.4.5 Composition dependence of the memory width of La doped Fe_2O_3 thin film device.

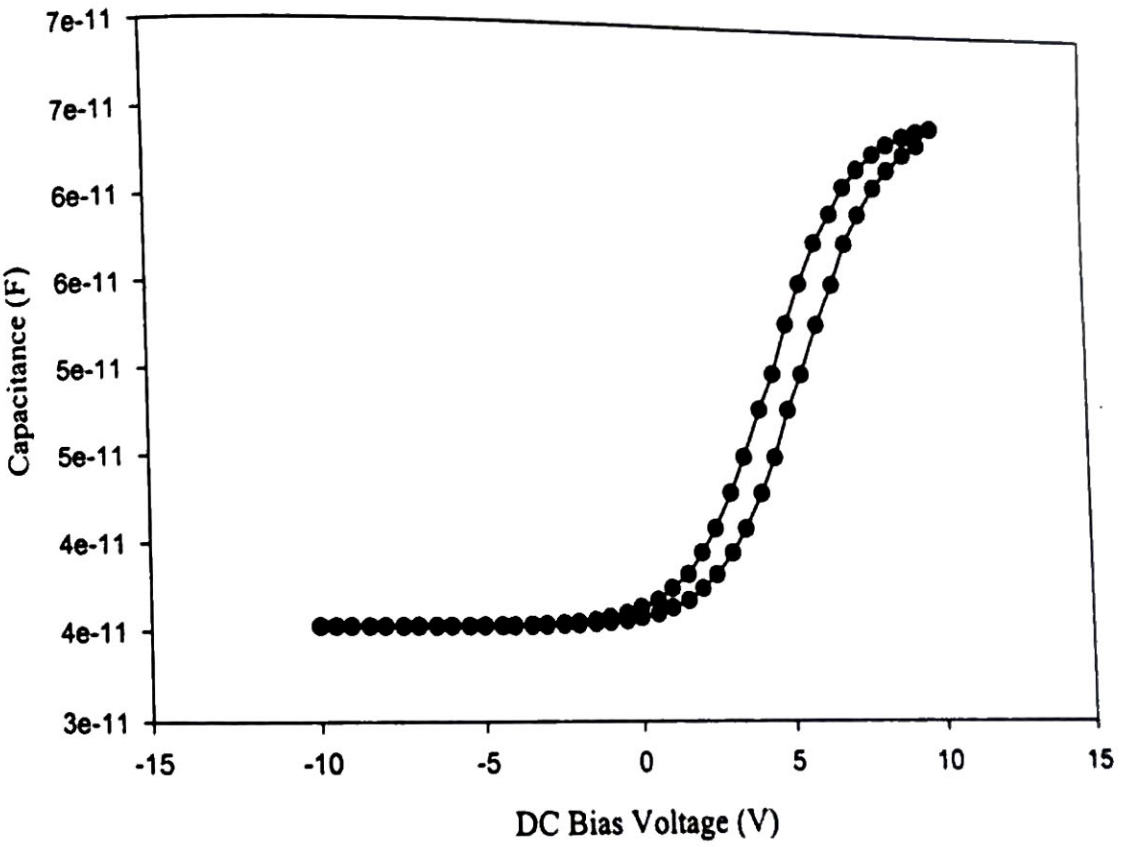


Fig. 4.6(a) Capacitance -Voltage characteristics of the La doped Fe_2O_3 (x =0.02) thin film device formed by annealing at 600^oC.

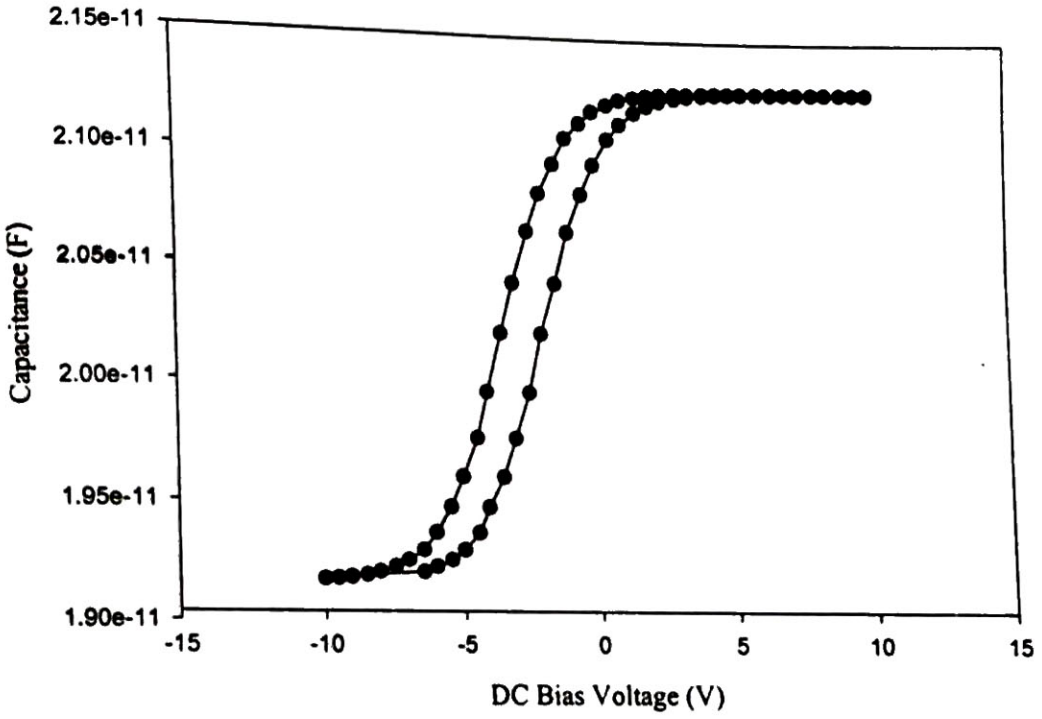


Fig.4.6(b) Capacitance -Voltage characteristics the La doped Fe_2O_3 (x=0.04) thin film device formed by annealing at $600^{O}C$.

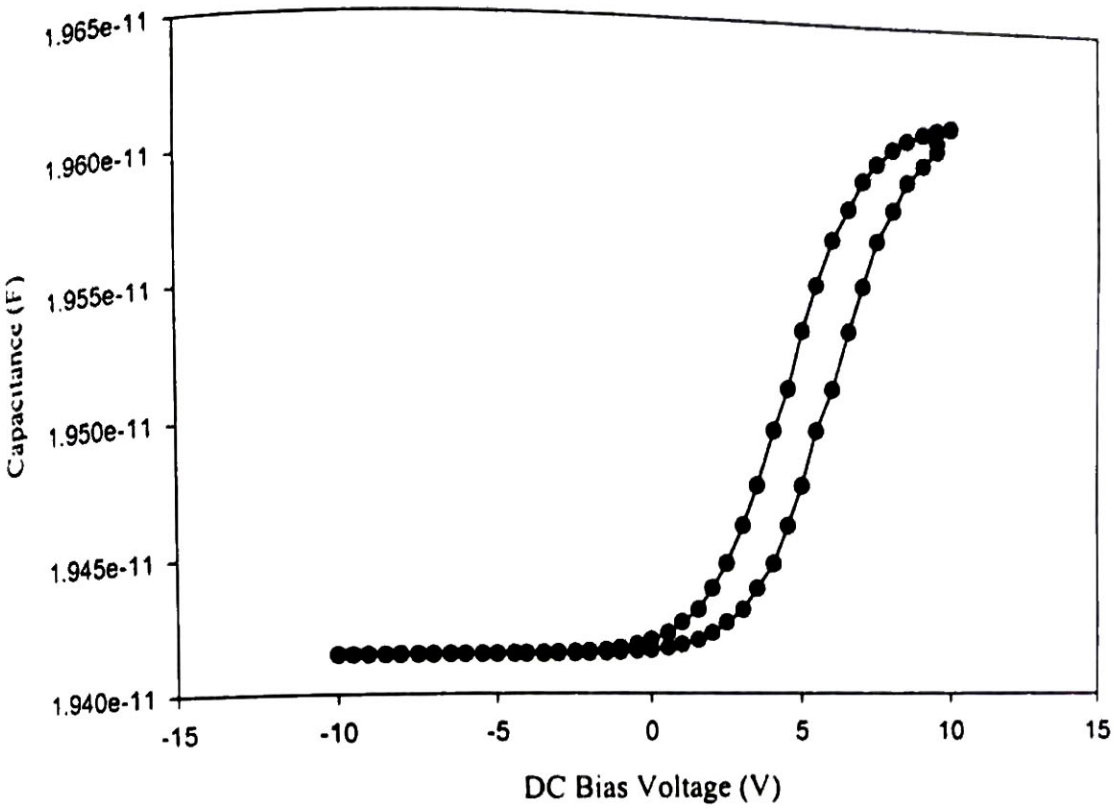


Fig.4.6(c) Capacitance -Voltage characteristics of the La doped Fe_2O_3 (x =0.06) thin film device formed by annealing at $600^{o}C$.

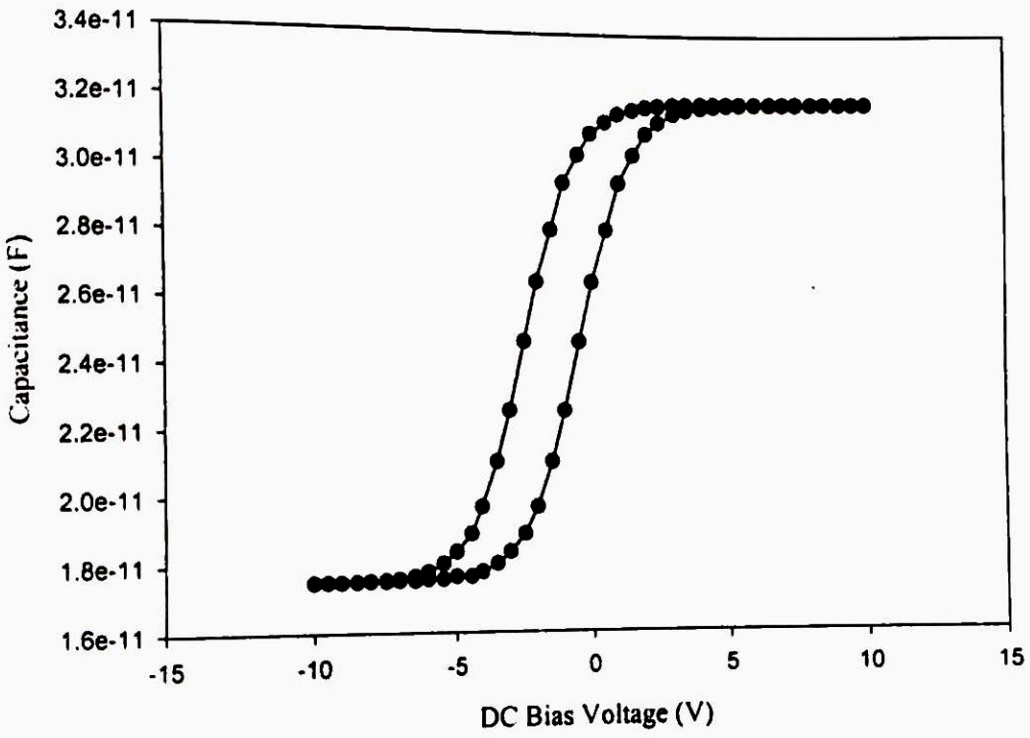


Fig.4.6(d) Capacitance -Voltage characteristics of the La doped Fe_2O_3 (x =0.08) thin film device formed by annealing at 600^oC.

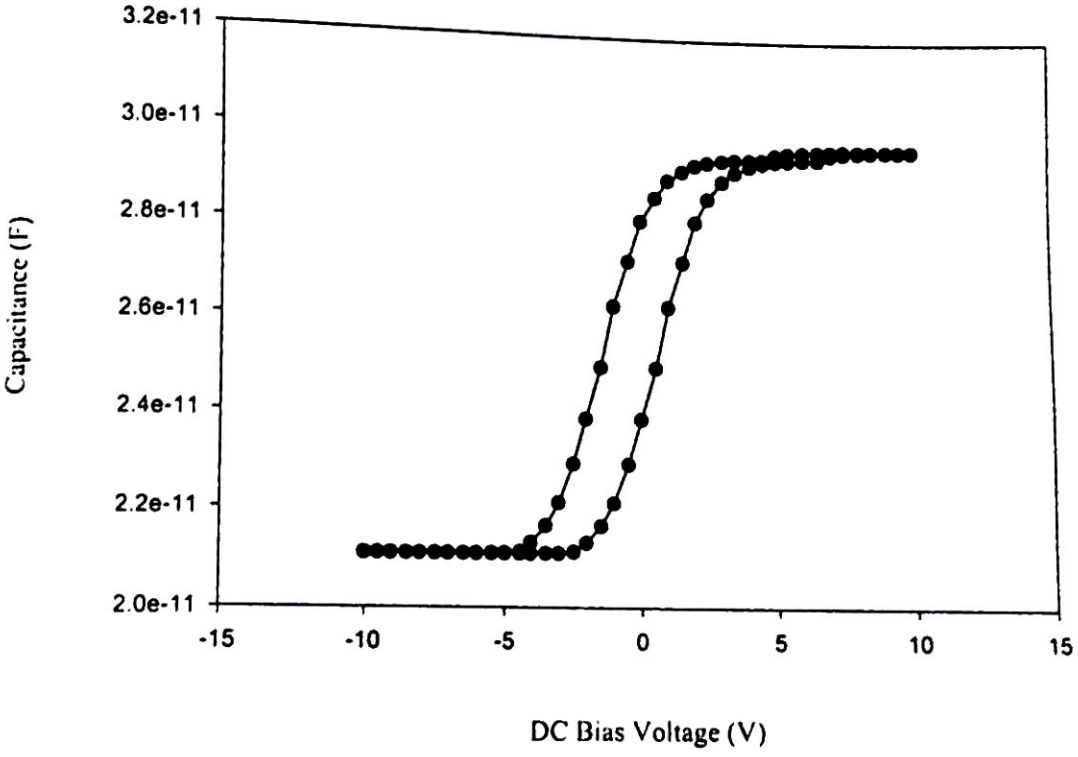


Fig.4.6(e) Capacitance -Voltage characteristics of the La doped Fe_2O_3 (x =0.10) thin film device formed by annealing at $600^{o}C$.

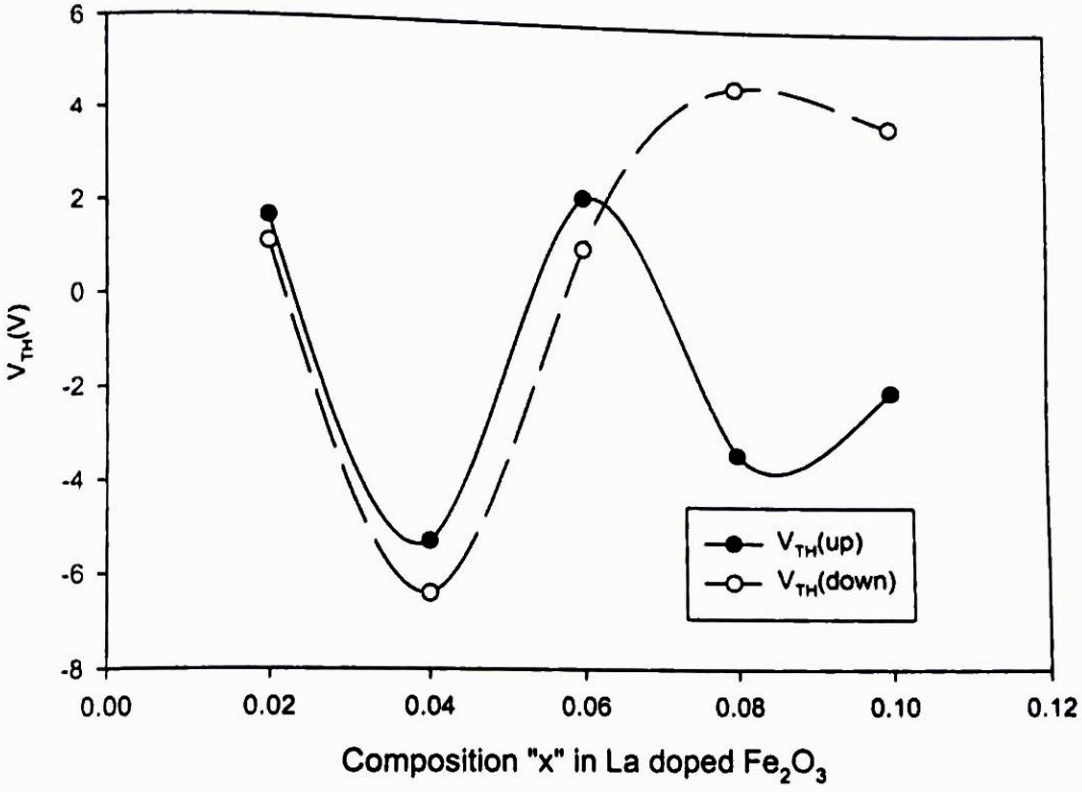


Fig .4.7 Composition dependence of the Threshold voltage of La doped Fe_2O_3 thin film capacitor.

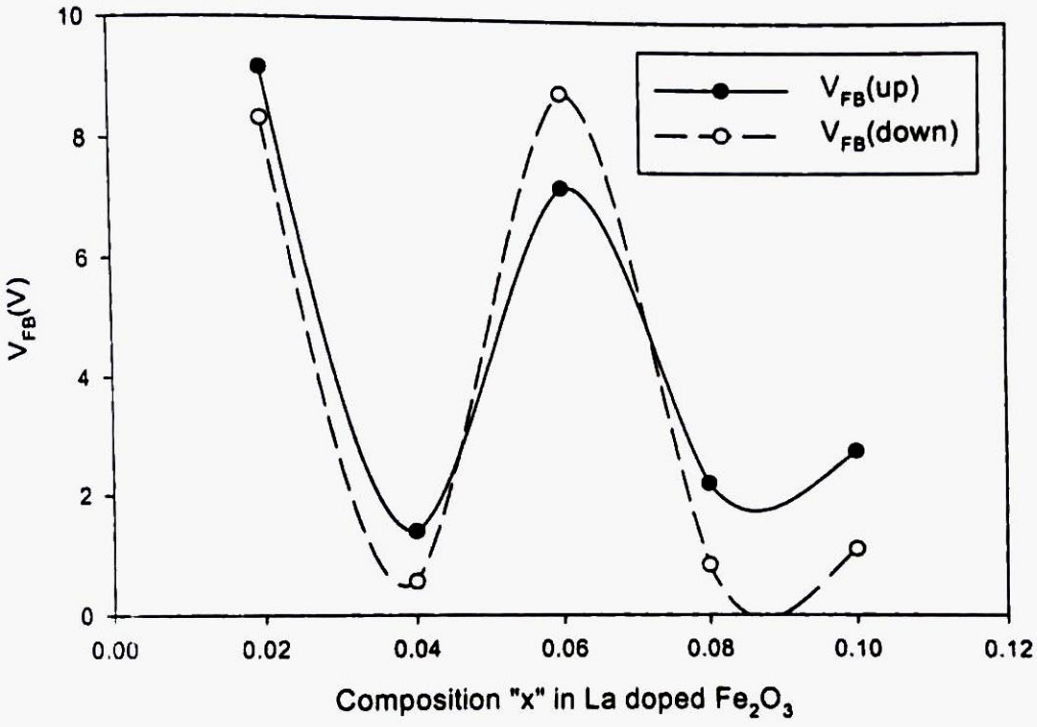


Fig. 4.8 Composition dependence of the flat band voltage of La doped Fe_2O_3thin film capacitor.

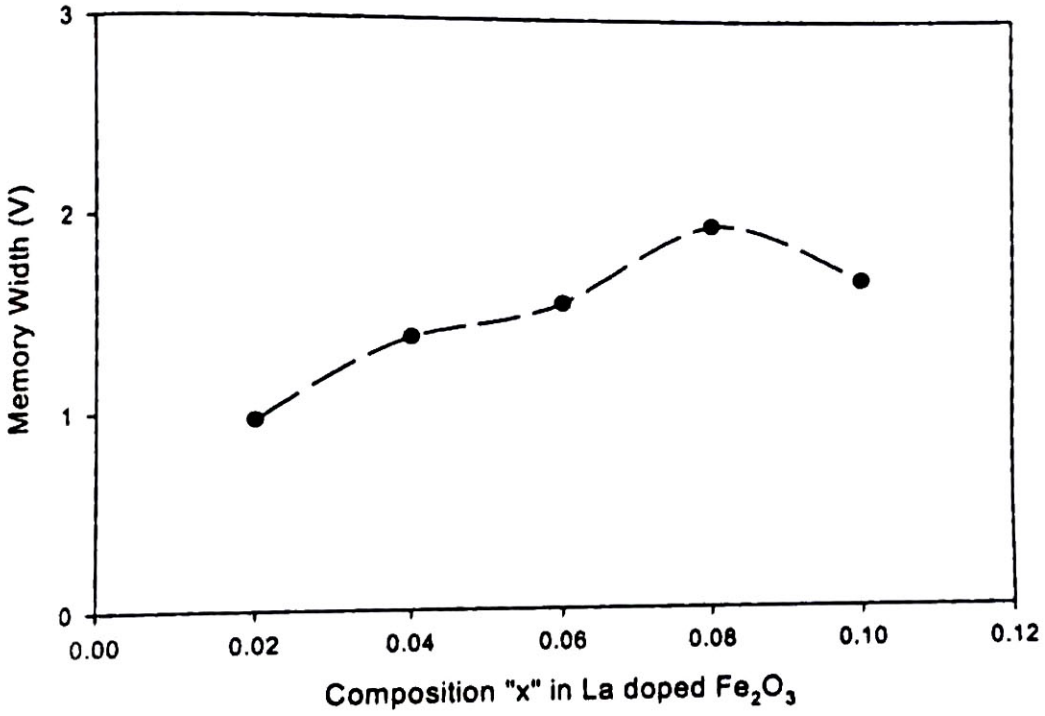


Fig.4.9 Composition dependence of the memory width of La doped Fe_2O_3 thin film capacitor.

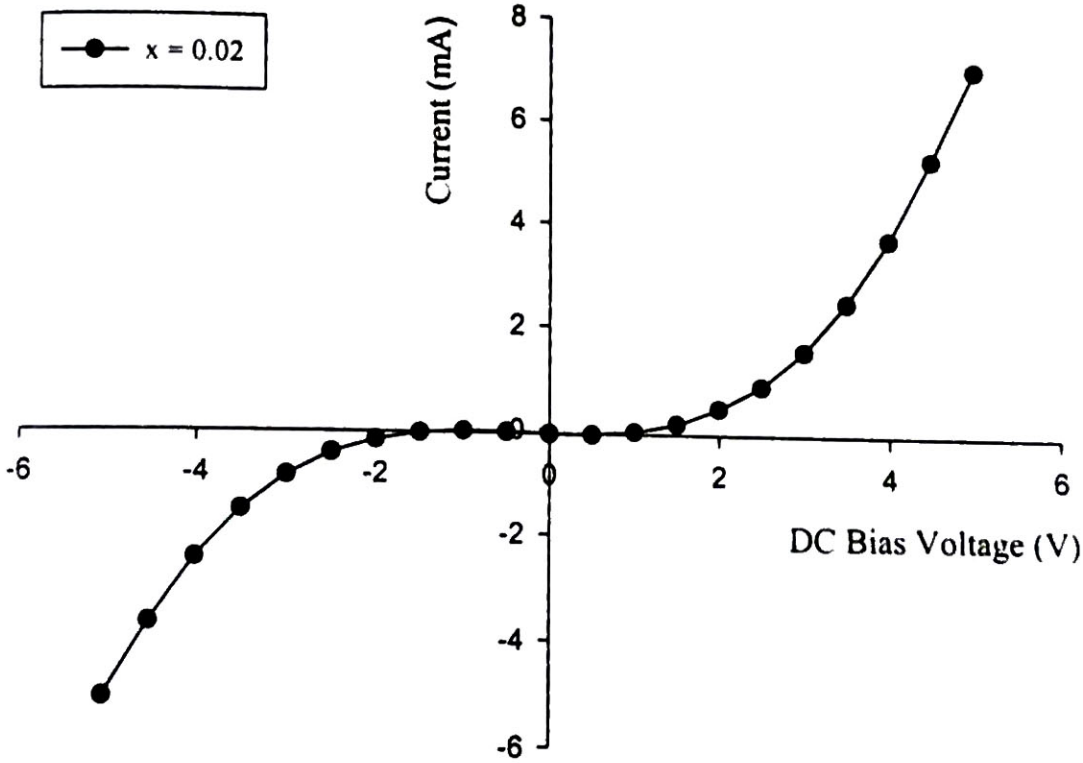


Fig.4.10(a) I-V characteristics of La doped Fe_2O_3 thin film (x = 0.02) formed at 600^{o}C.

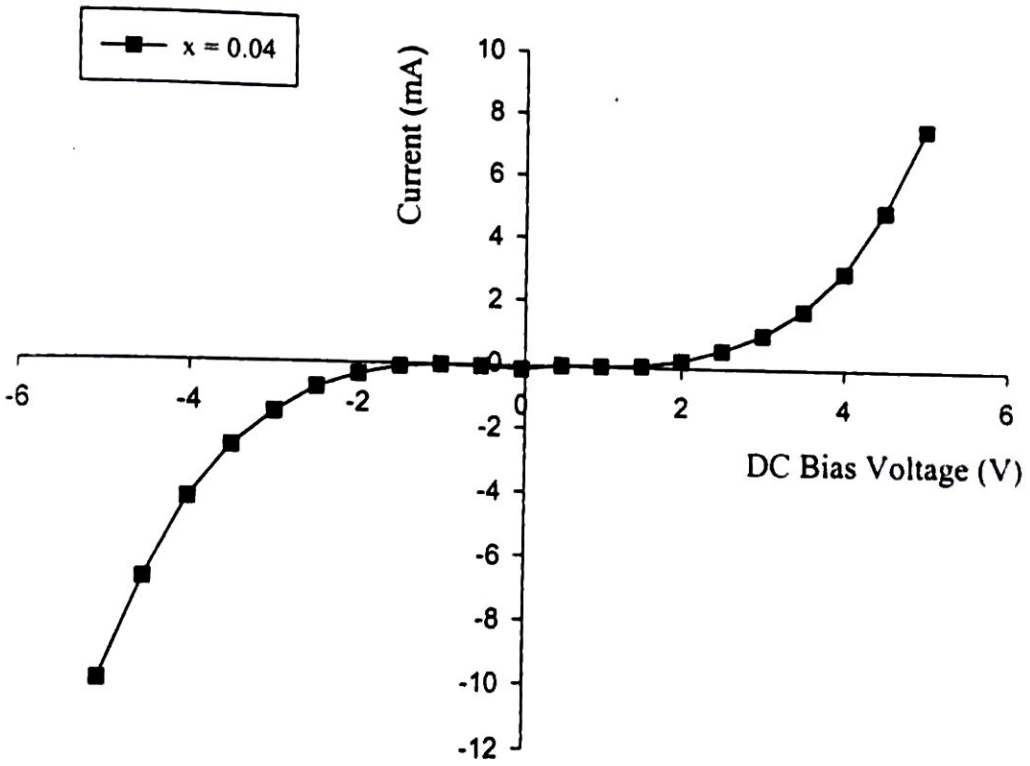


Fig.4.11(b) Ln I vs. V Characteristics of La doped Fe2O3 thin film device (x = 0.04) formed at 600°C

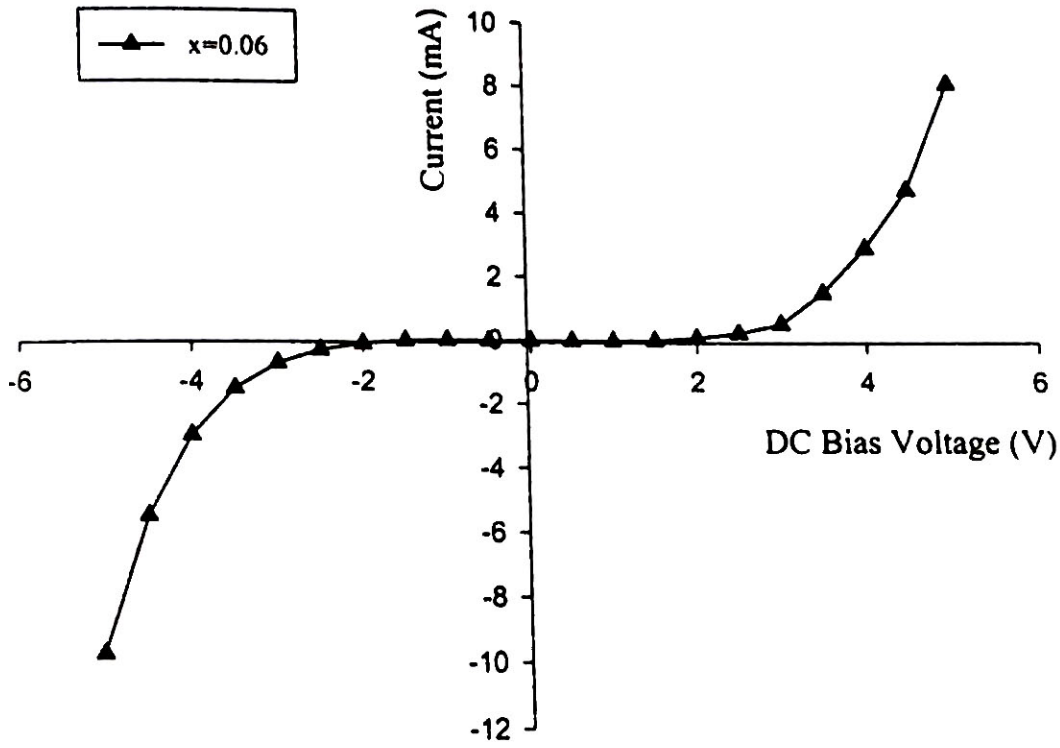


Fig.4.10(c) I-V characteristics of La doped Fe_2O_3 thin film (x = 0.06) formed at 600^oC.

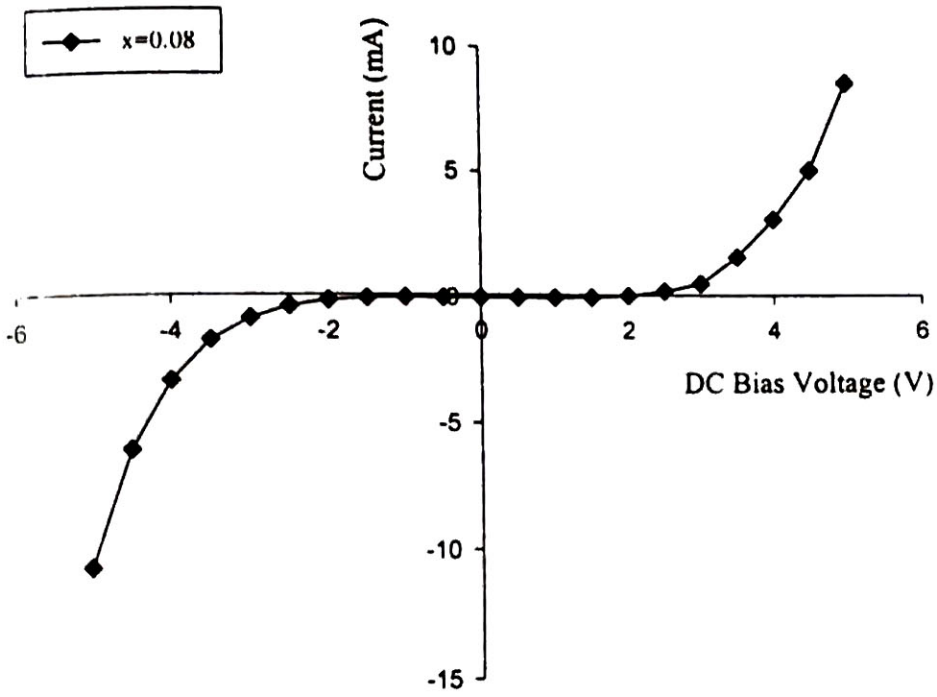


Fig.4.10 (d) I-V charachterisitcs of La doped Fe_2O_3 thin film (x = 0.08) formed at 600°C

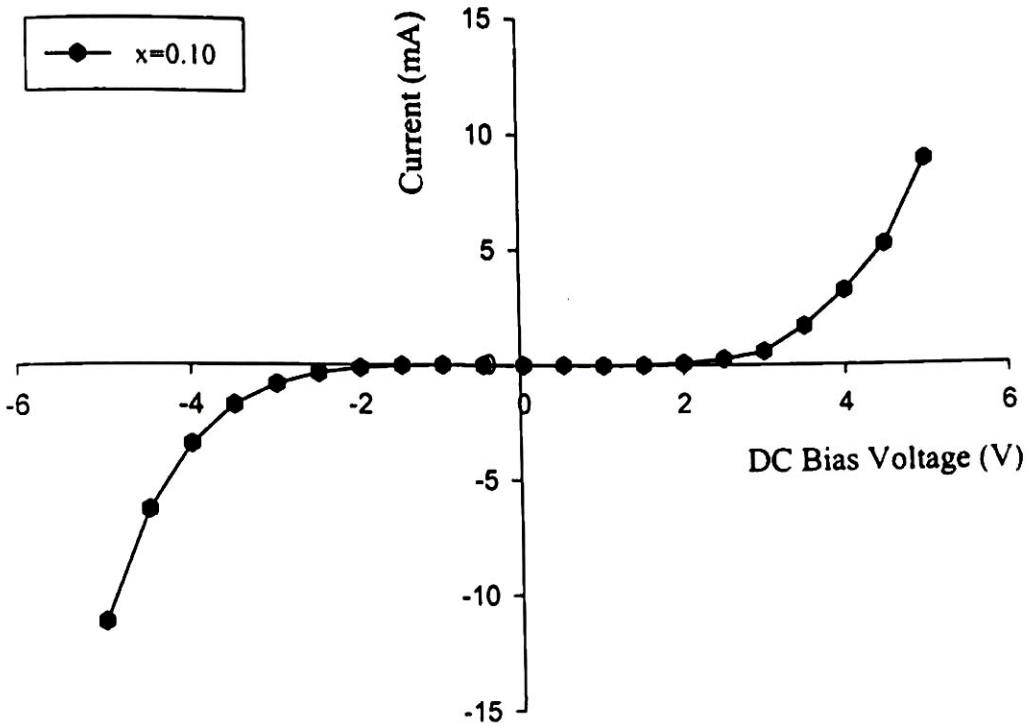


Fig.4.10(e) I-V characteristics of La doped Fe_2O_3 thin film (x = 0.1) formed at $600^{o}C$.

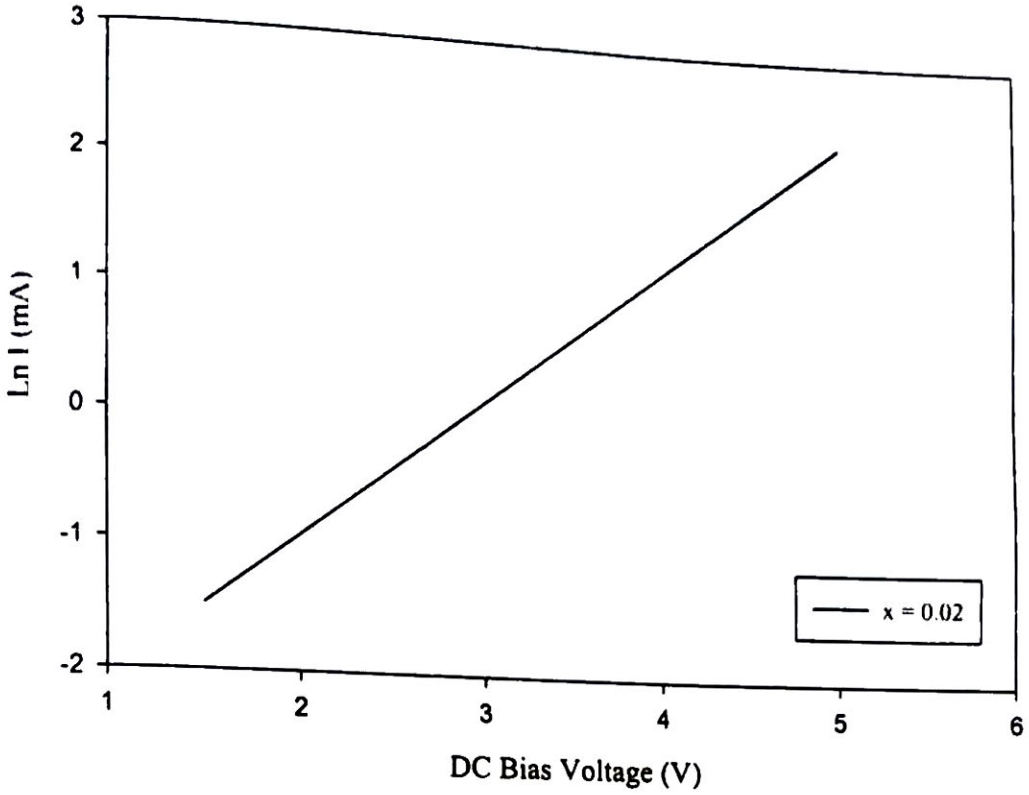


Fig.4.11(a) Ln I vs. V characteristics of La doped Fe_2O_3 thin film device (x = 0.02) formed at 600^{o}C.

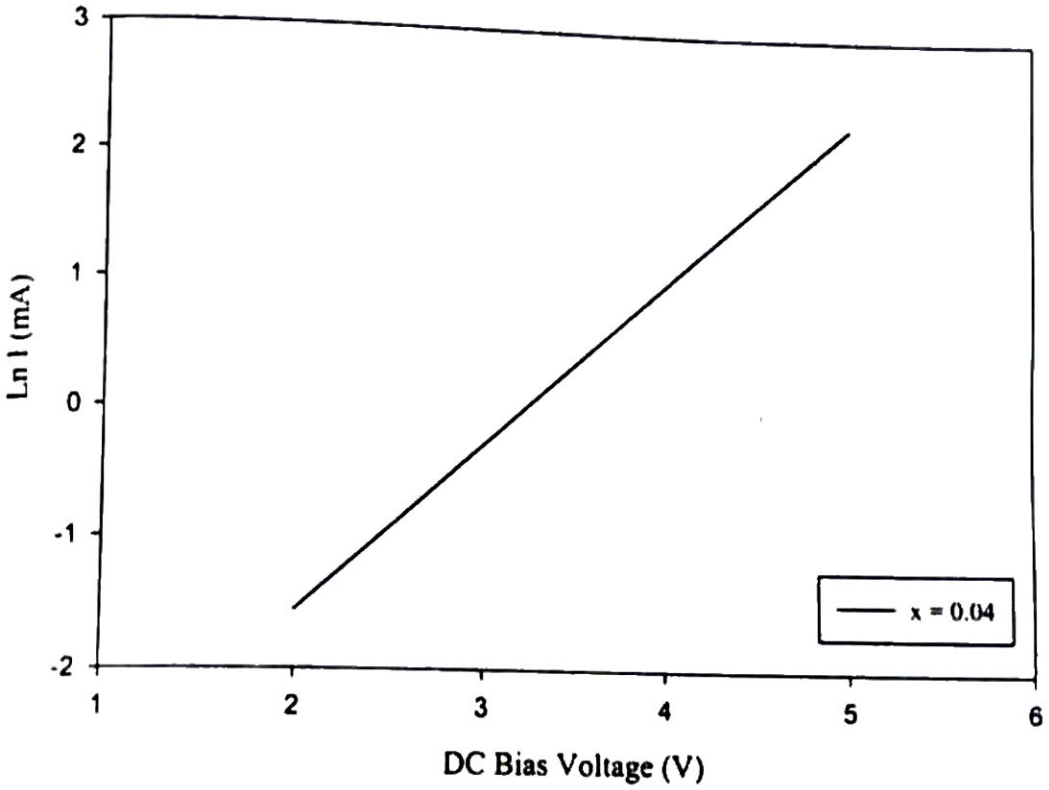


Fig.4.11(b) Ln I vs. V characteristics of La doped Fe_2O_3thin film device (x = 0.04) formed at 600^{o}C.

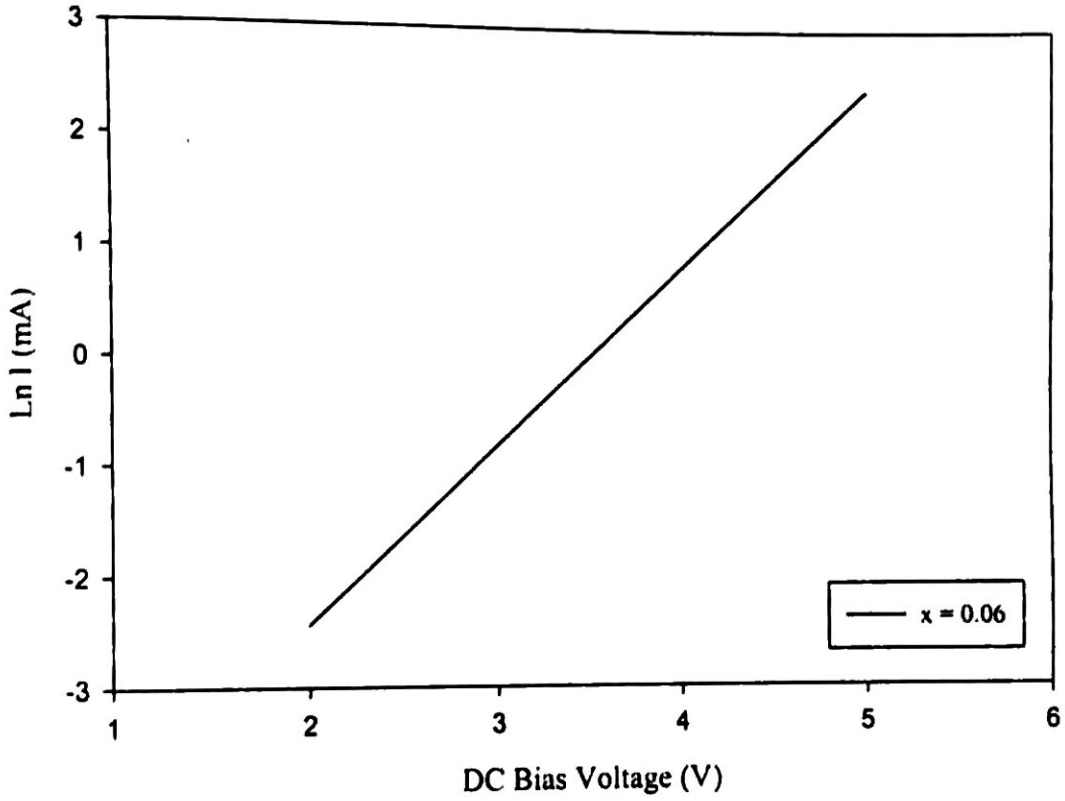


Fig.4.11(c) Ln I vs. V characteristics of La doped Fe_2O_3 thin film device (x = 0.06) formed at $600^{o}C$.

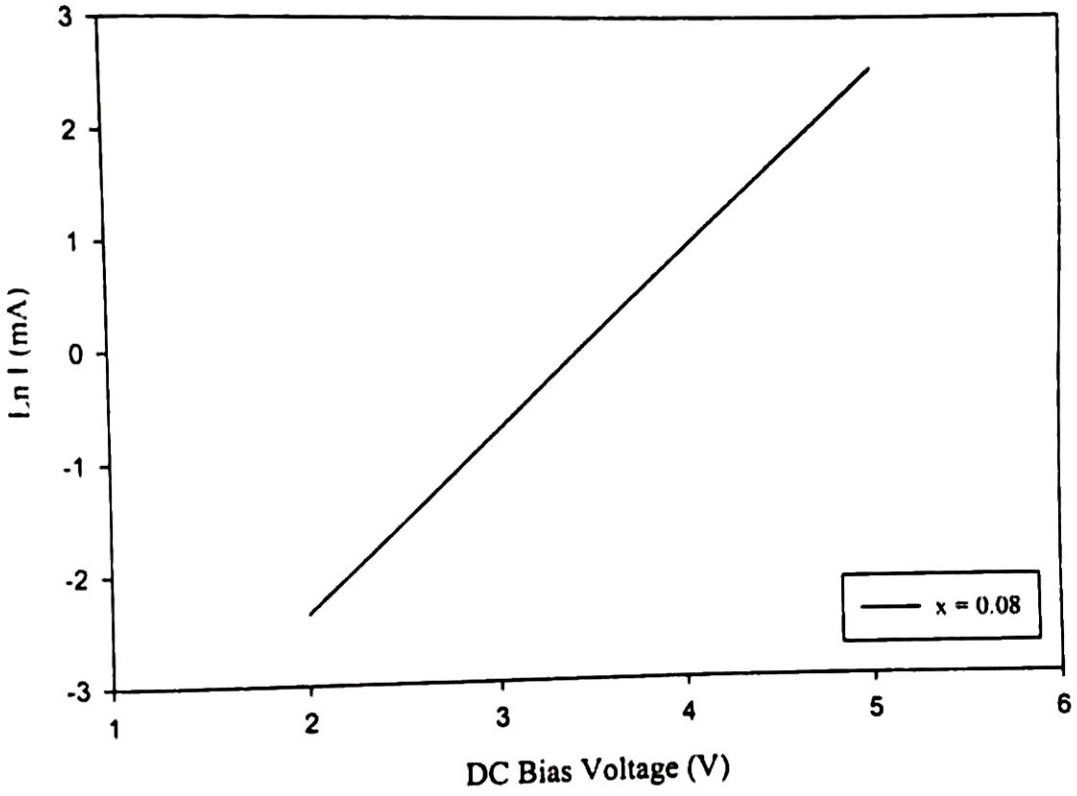


Fig.4.11(d) Ln I vs. V characteristics of La doped Fe_2O_3thin film device (x = 0.08) formed at 600^{o}C.

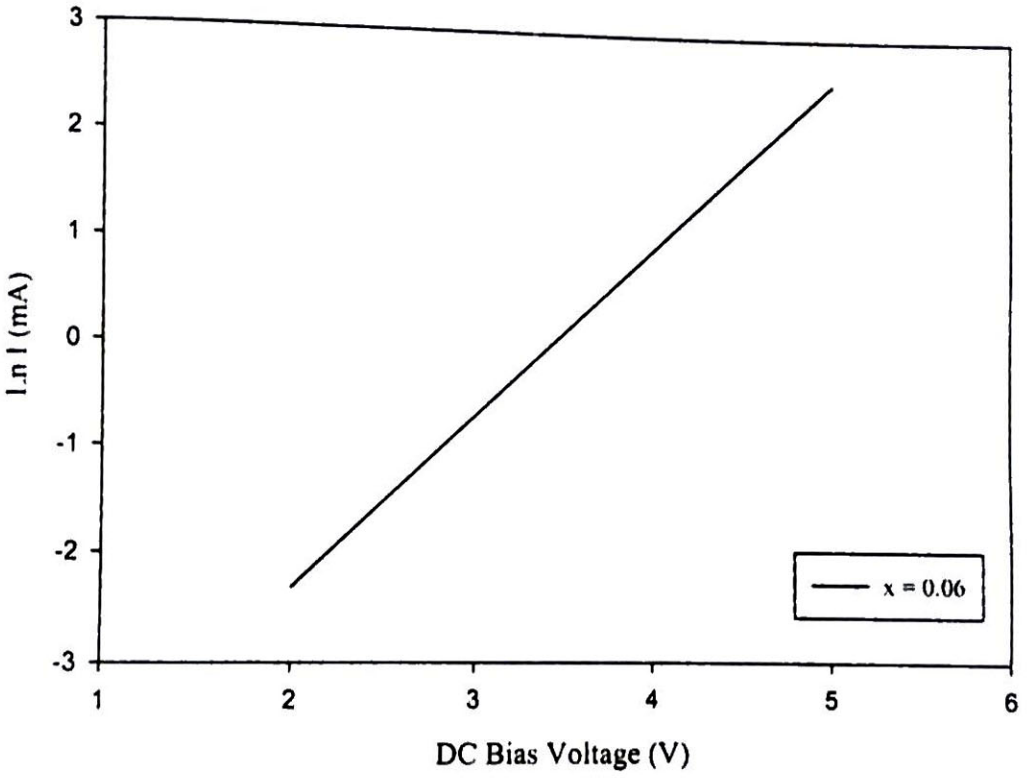


Fig.4.11(e) Ln I vs. V characteristics of La doped Fe_2O_3thin film device (x = 0.10) formed at 600^oC.

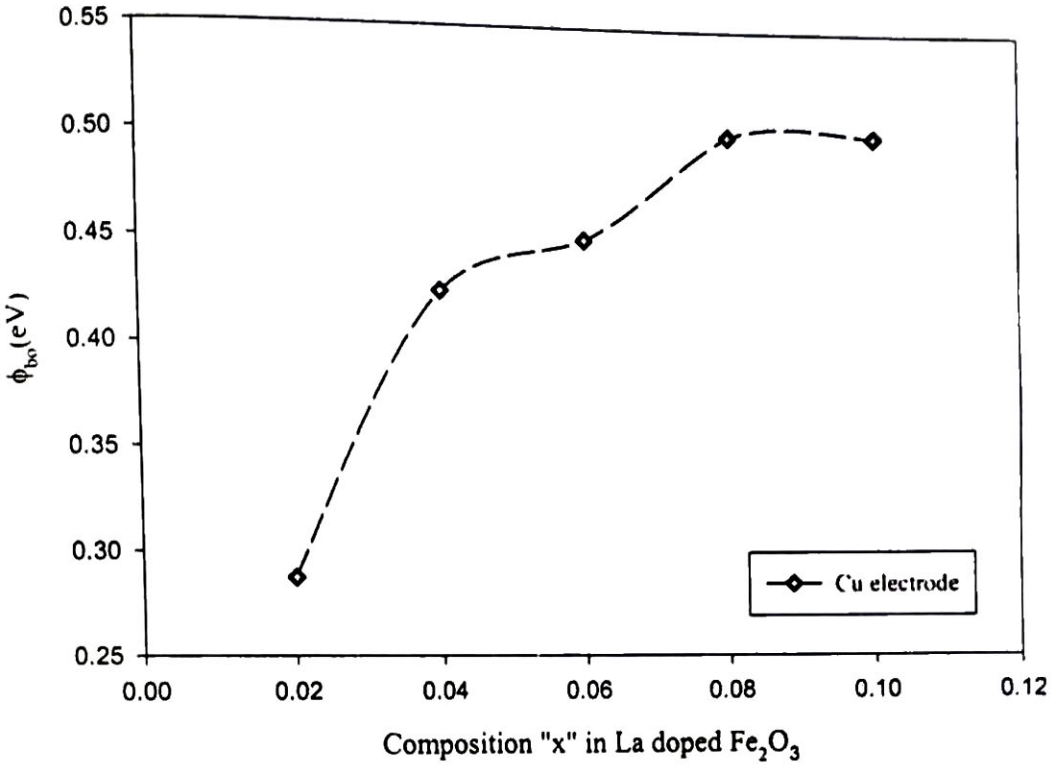


Fig.4.12 Composition dependence of the zero-bias barrier height of La doped Fe_2O_3 thin film device.

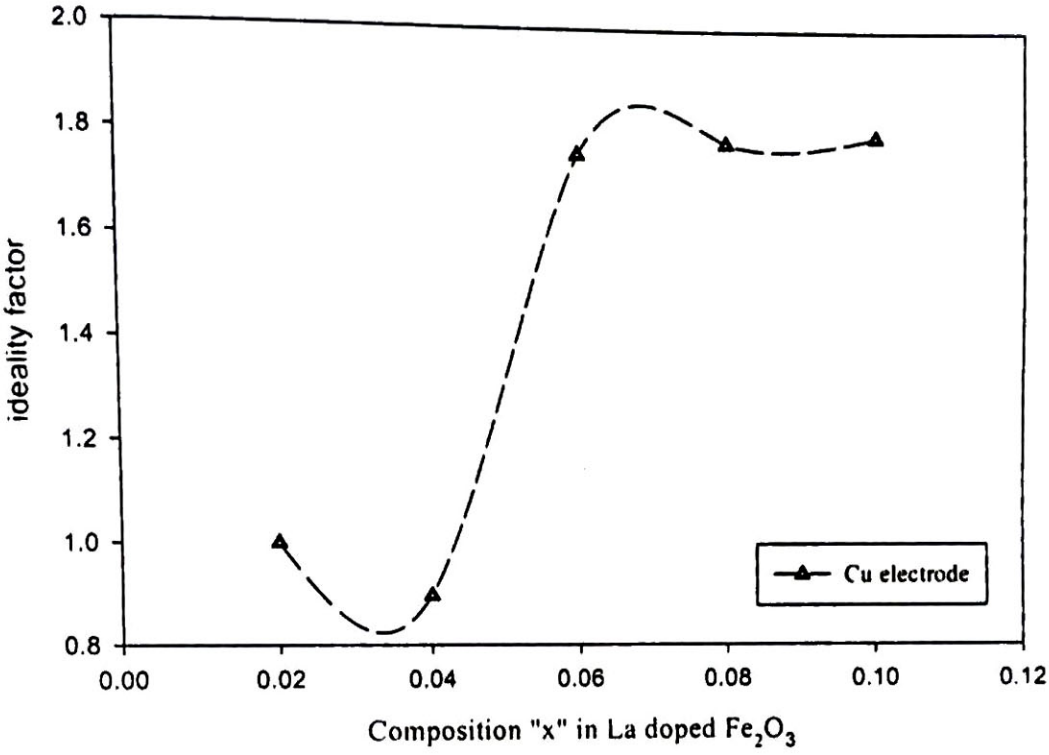


Fig.4.13 Composition dependence of the ideality factor of La doped Fe_2O_3 thin film device.

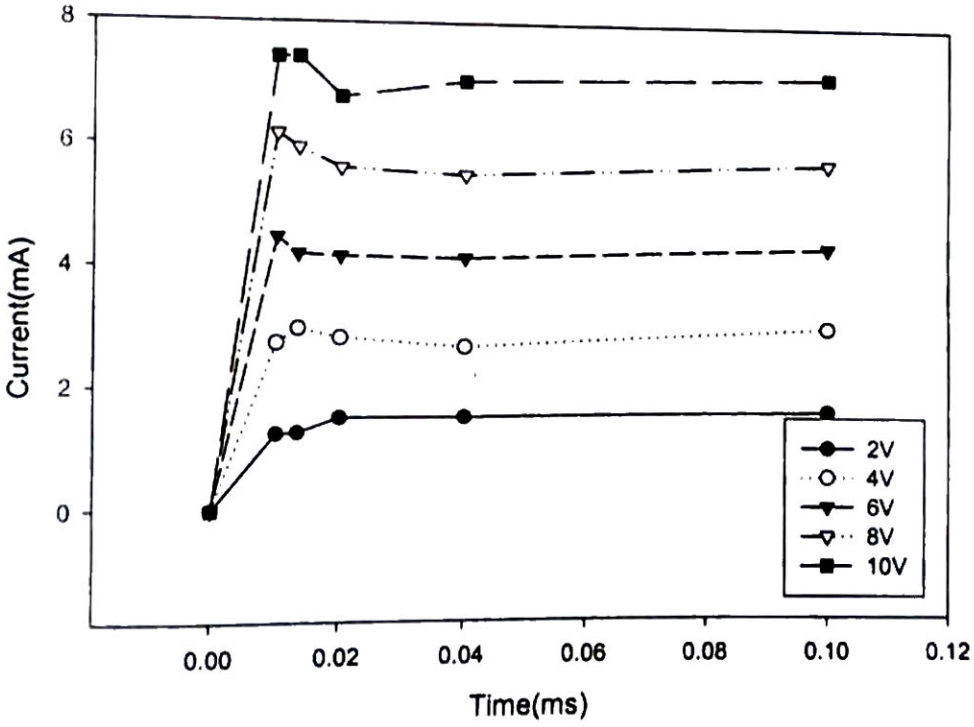


Fig. 4.14 (a) Transient current - time curve measured with La doped Fe_2O_3 (x=0.02) thin film capacitor (formed at 600^{o}C) for Cu electrode.

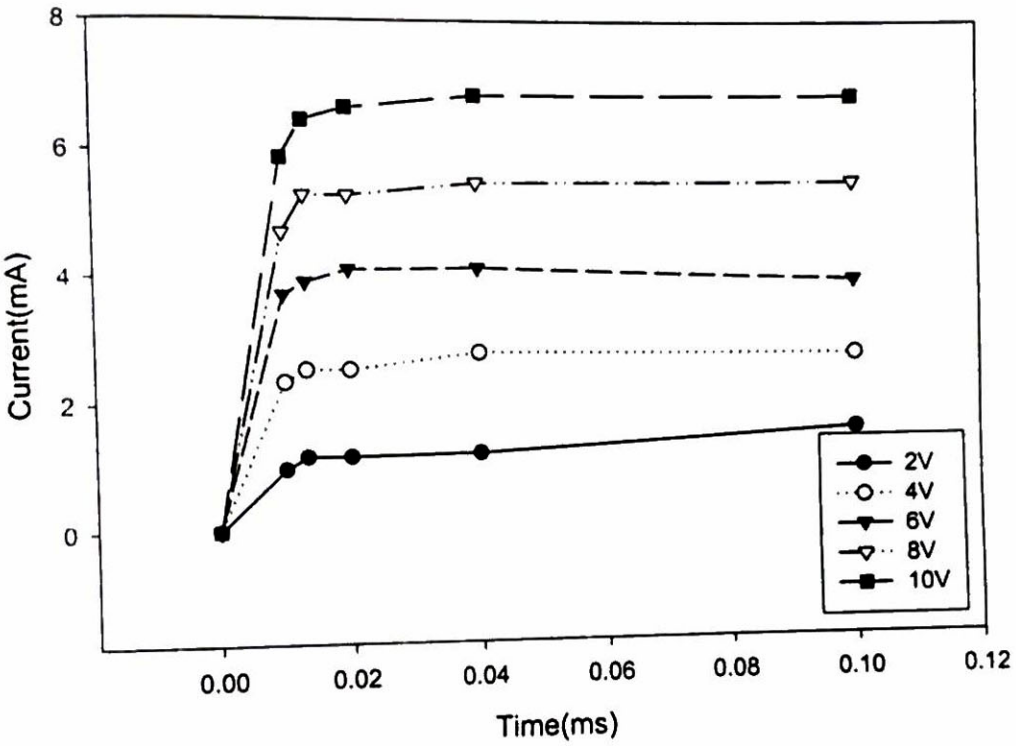


Fig. 4.14(b) Transient current - time curve measured with La doped Fe_2O_3 (x=0.04)thin film capacitor (formed at 600^oC) for Cu electrode.

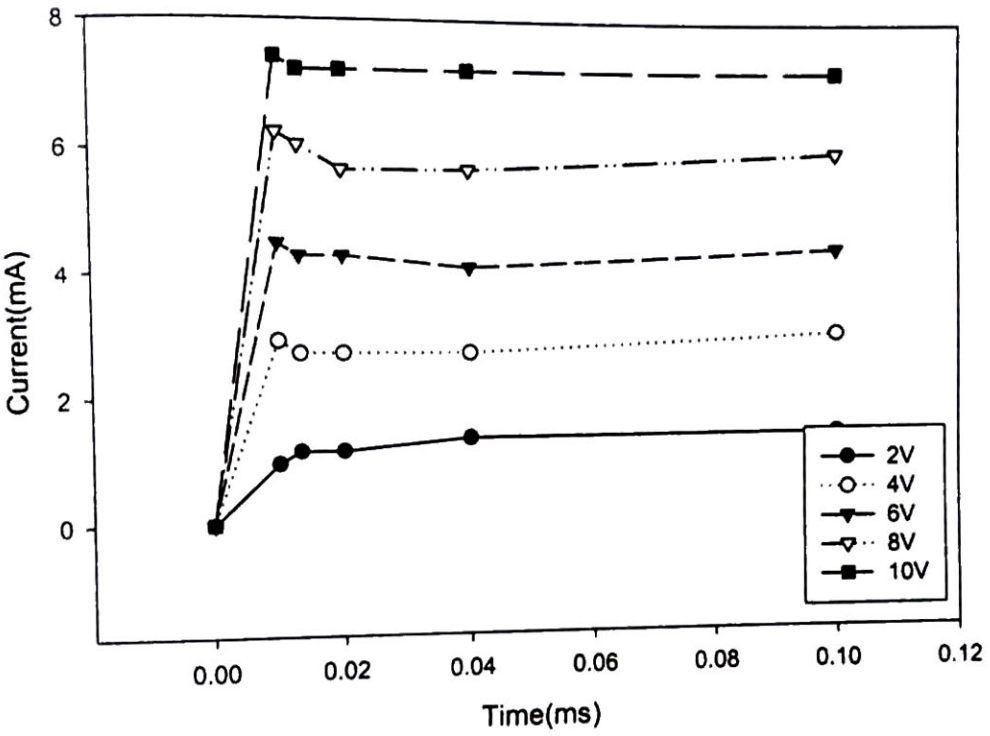


Fig. 4.14(c) Transient current - time curve measured with La doped Fe_2O_3 (x=0.06) thin film capacitor (formed at 600^{o}C) for Cu electrode.

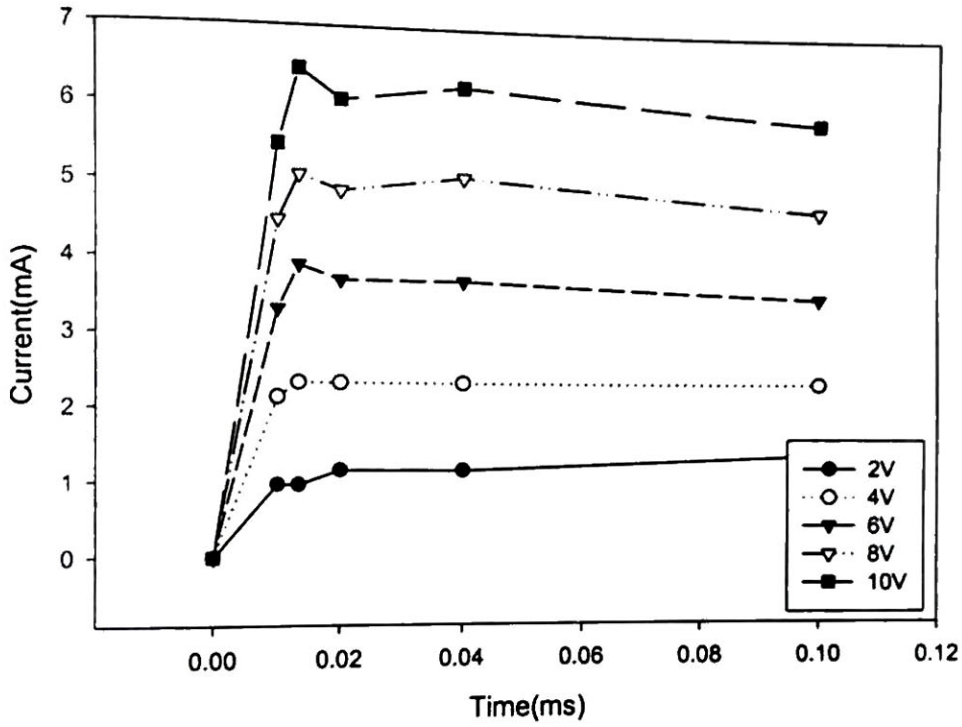


Fig.4.14 (d) Transient current - time curve measured with La doped Fe_2O_3 (x=0.08) thin film capacitor (formed at 600^{o}C) for Cu electrode.

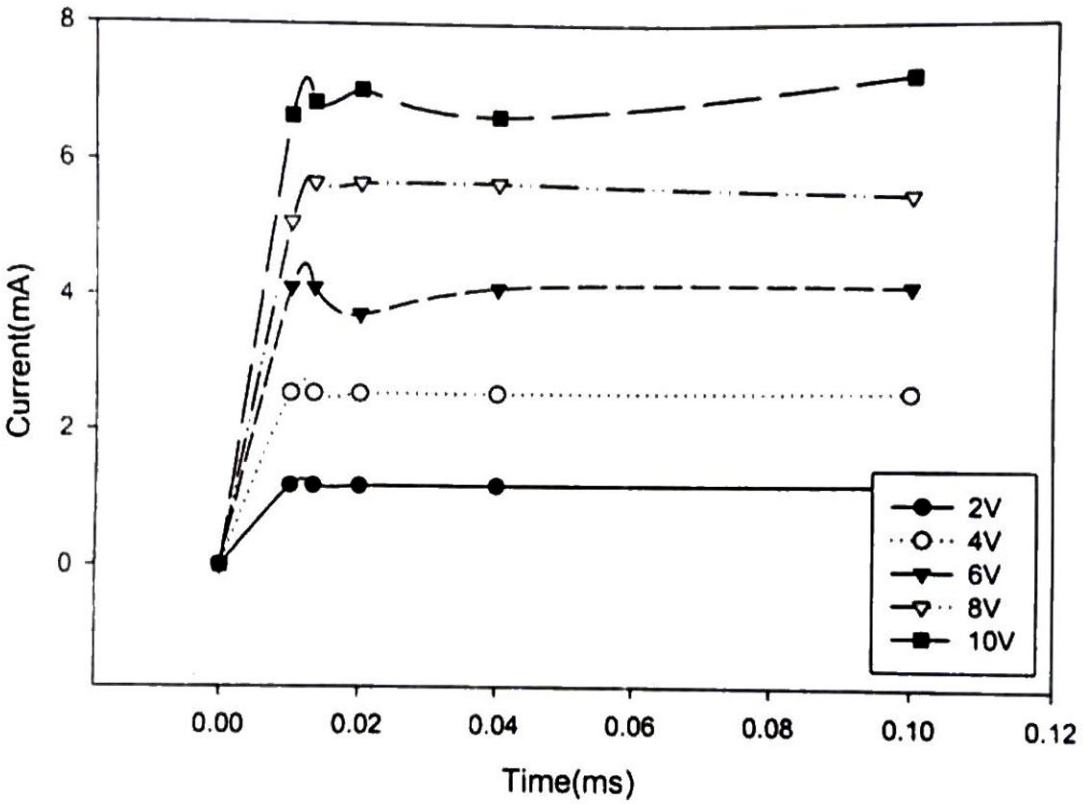


Fig. 4.14 (e) Transient current - time curve measured with La doped Fe_2O_3 (x=0.10) thin film capacitor (formed at 600^oC) for Cu electrode.

CHAPTER V
CONCLUSION

Fabrication and characterization of MFS multilayer configurations with ferroelectric La doped ion (III) oxide thin films have been investigated. The results calculated from ferroelectric electrical characterizations, the choice of material system, fabrication technique and multilayer design in this study are promising for memory device technology.

The memory window estimated from capacitance and voltage characterization measurement, it is clearly suggested that the influence of modification material into ion (III) oxide films due to the wider value of window. This value implies that our fabricated MFS devices in all cases are applied to FET memory technology. From C-V curve (Swept up and Swept down), moreover, it is found that the ferroelectric materials in this work can control the Si-surface potential and this fact can be also applied to MFSFET devices. On the other hand, the dopant materials into ion (III) oxide are helpful to increase the memory window and can decide that all devices with MFS designs are possible to nonvolatile FET applications.

The most important nonvolatile memory technology, hysteresis parameters obtained from loops are suitable for thin film integration into ferroelectric memory devices. The remanent polarization gradually increases when applied voltage is raised in La doped Fe_2O_3 films.

Our result on the charging current of La doped Fe_2O_3 capacitors as a function of time (I-t curves) measured at room temperature with 10V is reported. In our experiment, an Cu/La doped Fe_2O_3 / n-Si is used at 10 bias voltages and transient

current increases with time. The increase of transient current at high voltage is most likely due to the trapping holes. The accumulation of trapped holes causes an enhancement of the local electric field in the film, thus increasing the conduction current. This type of transient current behavior is designated as "degradation type". The obtained results in this work indicated that the MFS design memory devices could be applied to nonvolatile memory device applications.

Therefore, various modifications into ion (III) oxide been studied with the aim of obtaining of improved properties to make them potential useful in practical application. The present results in this research indicate our fabricated memory devices with new sol-based method are very promising candidates for memory device applications.

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