Fabrication and Characteristics of SnO_2/PZT/SiO_2/p-Si Ferroelectric Memory Structure

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***Abstract*— Metal-Ferroelectric-Insulator-Semiconductor Structures are fabricated and characterized by using Pb(Zr,Ti)O_3(PZT)and SnO_2 layers. Ferroelectric PZT layers are formed on SiO_2/p-Si by the spray method and SnO_2 layers are deposited on PZT/SiO_2/ p-Si structure by spinning technique. The capacitance-voltage(C-V) characteristics of the SnO_2/PZT/SiO_2/p-Si structure exhibit a hysteresis loop due to the ferroelectricity of the PZT layer. In the memory behaviour described in this paper, the transistor itself has memory; the transistor is capable of storing one bit of information.**

***Keywords*— Ferroelectric-Gate FET, Metal-Ferroelectric-Semiconductor (MFIS), SnO_2, Pb(Zr,Ti)O_3(PZT).**

I. INTRODUCTION

The ability to store information is an important requirement in a digital system. Circuits and systems designed specifically for data storage are referred to as memory. In a larger system, such as a microcomputer, the memory may be compound of semiconductor memory chips. Semiconductors in the memory field replaced instead of magnetic due to the speed, density, cost and power advantages. When the gate electrode of a conventional MOSFET is modified so that semipermanent charge storage inside the gate is possible, the new structure becomes a nonvoltatile memory device. Since the first nonvolatile memory device proposed by Kahng and Sze in 1967, various device structures have been made, and nonvolatile memory devices have been extensively used in integrated circuits such as the electrically alterably-read only memory(EAROM), the erasable-programmable-read only memory (EPROM)and nonvolatile random access memory (NVRAM).

Devices physics and fabrication technologies regarding to ferroelectric thin films have been received much attention for the past decade and now, many achievements realized the practical application of the ferroelectric thin film in a VLSI memory and sensor. Ferroelectric memories have been evaluated for use in two different types of memories. One has a memory cell consisting of one transistor and one capacitor (1T1C) like a dynamic random access memory(DRAM). Another has a ferroelectric layer embedded in a metal-insulator-semiconductor field effect transistor (MFS-FET). MFS-FET offers several benefits such as long read/write cycles, simple circuit, long retention time, and high at low voltage. However, there is a fatal drawback to MFS-FET because the unwanted SiO_2 and the interfacial layer can be formed between the ferroelectric thin film and the substrate while depositing the ferroelectric thin film on the semiconductor substrate. When a gate voltage is applied to this thin SiO_2, thin oxide turns a moderate gate voltage into a high electric field that causes severe stress and high interface trap charges in the SiO_2. As a results, ferroelectric properties of MFS-FET might be regarded by the low dielectric SiO_2 layer. The conventional MFS structure has several problems. It is difficult to deposit ferroelectric thin film directly on a Si substrate. Pb, Ti and other elements diffuse into the Si substrate, and unnecessary SiO_2 layers are formed during thermal treatment. To solve these problems, a buffer layer between the silicon and the ferroelectric layer has been considered. By inserting an insulator such as MgO, CeO_2, ZrO_2 and $SrTiO_2$, a MFS-FET changes into a MFIS-FET and charge injection phenomena on the SiO_2 layer can be prevented by the voltage distribution relationship among the ferroelectric, insulator and native SiO_2.

In this paper, PZT(lead zirconate titanium) is used as ferroelectric layer. PZT is one of the most widely studied ferroelectric materials due to its higher permittivity, higher remanent polarization and lower coercive field. SnO_2 (Tin Oxide) is also used as transparent conducting oxide. The

MFIS- FET using a Cu/SnO_2/PZT/SiO_2/p-Si structure have been fabricated and determined electrical properties and ferroelectric behavior of the MFIS-FET.

II. Experimental Procedures

The n- channel MOS-FET was fabricated on p-type Si (100) wafers by conventional technique. The first step is to create a thin layer of silicon dioxide (SiO_2) layer on the surface of a Si-substrate by thermal oxidation. The next step in the process is to deposit a wax coating on top of the SiO_2 layer to create the windows. The windows are opened by applying dilute hydrofluoric acid solution ($HF:H_2O$=1:5) and acetone. The acid etches away the SiO_2 layer. After that, the structure is ready for the impurity diffusion process. The source and drain are defined by implanting P (phosphorus)ions through the windows into the silicon crystal. The depth of phosphorus penetrates and its concentration(doping density) depend on the temperature of the process and the length of time it is allowed to occur. To fabricate the MFIS-FET, the oxide layer on top of the gate channel region is also removed, and PZT layer was formed on gate oxide of the structure by using spray coating techniques. The prepared PZT layer are annealed at 800°C for one hour. SnO_2 layer are prepared by sol gel method on the PZT/SiO_2/p-Si gate channel region. SnO_2 are deposited by spinning technique with 1000rpm and annealed at 700°C for 30 min in the furnace. Capacitance-voltage(C-V) and current-voltage (I-V) are measured. Polarization-electric field(P-E) characteristic is also tested.

III. Results and Discussion

Figure 1 illustrates drain characteristic of fabricated n Channel MISFET structure which is prepared under 600 °C annealing temperature, with the gate voltage descending from 10V to 2V in 2V intervals. Note that the device operates in enhancement mode. Figure 2 depicts transfer characteristic of above n- channel MISFET structure. Conduction of leakage current rapidly increased through the voltage range of 3V to 10V. The curve has an ohmic conduction region in which the current linearly increasing with applied voltage. Ohmic region has a transition voltage V_t around 3V from which linear relation in current versus voltage begins. Figure 3 shows the I_D-V_G characteristic of SnO_2/PZT/SiO_2/p-Si structure. The voltage is varied first from 0V to + 10V, then from + 10V to -10 V, and finally from +10V to 0V at a step of 1V. The result in figure shows that the current still have in V_{GS}= 0V and nearly constant in negative bias conductions. It is investigated a hysteresis loop behaviors. Note that the hystersis in the trancondauctance curve indicates the memory window is about 3V.

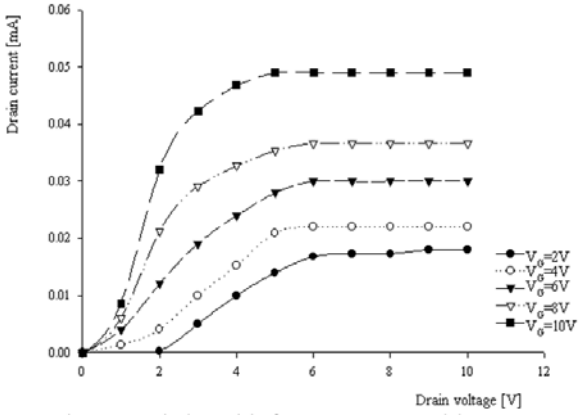

Figure 1 Drain Characteristic of MISFET Structure

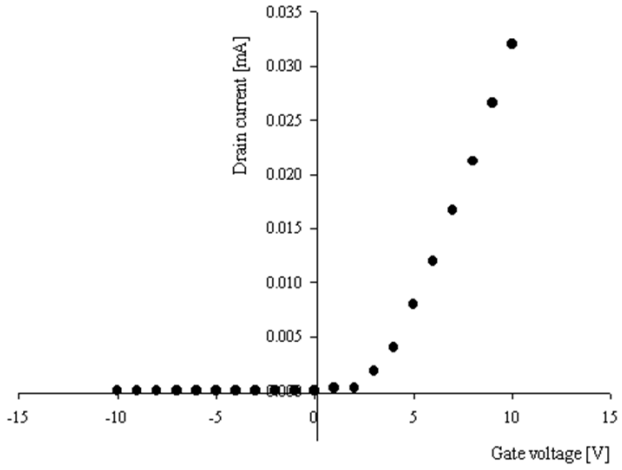

Figure2 Transfer Characteristic of MISFET structure

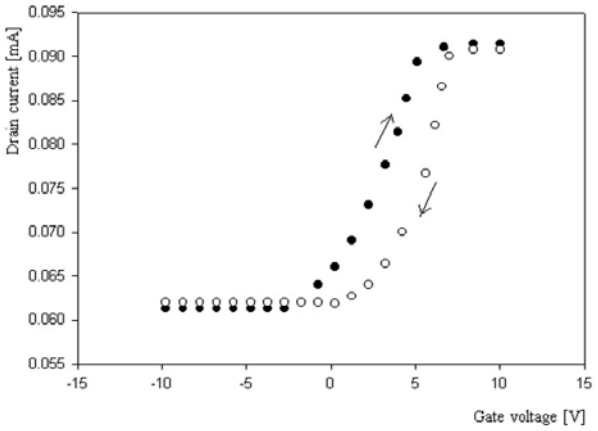

Figure 3 I_D-V_G Characteristic of Fabricated SnO_2/PZT/SiO_2/p-Si structure

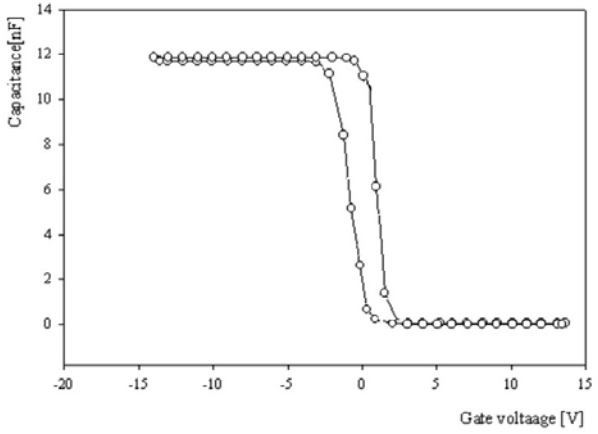

Figure 4 C-V Characteristic of Fabricated SnO_2/PZT/SiO_2/p-Si structure

CV characteristic at 100Hz in the region of -14V to +14V for SnO_2/PZT/SiO_2/p-Si structure is shown in figure 4. The flat band voltage(V_{FB}) and the threshould voltage(V_{TH}) in sweep up were -0.28V and 1.1V on the Si substrate. When the bias voltage has one cycle, the density of the interfacial surfaces states (N_{SS}) can be represented as

$$N_{SS} = C_a V_H / qA \qquad 1.1$$

Where C_a is capacitance in the accumulation region, q is charge, V_H is voltage width of hysteresis, and A is electrode area. N_{SS}, calculated from the hysteresis width of C-V curve, was 2.82×10^{13} eV^{-1} cm^{-2} at 100 kHz. As the figure shows, the curves early exhibit the regions of accumulation, depletion, and inversion. Also, it can be seen that there are exist C-V hystersis loops which reflect the ferroelectric nature of the films and are necessary to realize the memory function. The difference of the bias voltage near the flat- band capacitance (called the memory window of the hystersis loop) about 1.39V in the operation of ±14V.

Figure 5 illustrates the (P-E) characteristic of the fabricated SnO_2/PZT/SiO_2/p-Si structure. It is observed that the systematic hysteresis loop by using Sawyer-tower method. The spontaneous polarization (P_s) and the remanent polarization (P_r) values of this structure calculated from figure 5 are 82 μC/cm^2 and 41.02μC/cm^2, respectively.

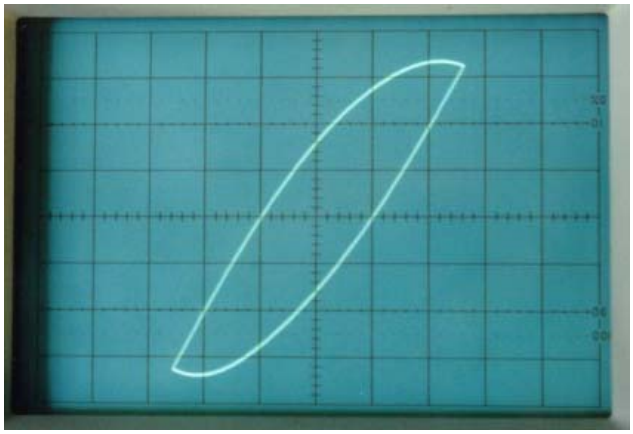

Figure 5 P-E Characteristic of Fabricated SnO_2/PZT/SiO_2/p-Si structure

VI. CONCLUSION

The experimental results of the research works can be summarized that PZT layer can be used as dielectric gate material for FeFET. Transparent conducting oxide SnO_2 , Tin Oxide is deposited on PZT layer also exhibits FeFET. SnO_2 layer has been successfully grown on PZT layer. SnO_2/PZT/SiO_2/p-Si structure has the memory windows effect. The results indicate that the SnO_2/PZT/SiO_2/p-Si structure are promising for application in memory devices and FETs, and also predict that these devices are used as light sensitive memory devices. On the basis of this research, it is intended to

use in IC manufacturing. Integrated circuit procedure needs detail study and experience. Therefore, if there is IC, Microprocessor manufacturing in semiconductor industries, I do believe that these experience and knowledge will be beneficial for useful and effective research projects in our country.

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Fabrication of $Pb(Zr,Ti)O_3$ Thin Film for Non-Volatile Memory Device Application

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Abstract*—Ferroelectric lead zirconate titanate powder was composed of mainly the oxides of titanium, zirconium and lead. PZT powder was firstly prepared by thermal synthesis at different Zr/Ti ratios with various sintering temperatures. PZT thin film was fabricated on SiO_2/Si substrate by using thermal evaporation method. Physical and elemental analysis were carried out by using SEM, EDX and XRD The ferroelectric properties and the switching behaviour of the PZT thin films were investigated.The ferroelectric properties and switching properties of the PZT thin film (near morphotropic phase boundary sintered at 800ºC) could function as a nonvolatile memory.

***Keywords*— lead zirconate titanate, thermal evaporation, SEM EDX , XRD ,coercive field , remanent polarization,transient current**

I. INTRODUCTION

Ferroelectric materials have (a) high dielectric constant (b) high piezoelectricity (c) relatively low dielectric loss (d) high electrical resistivity and (e) high electro-optic coefficients which make them attractive for a variety of application. Ferroelectric thin films ($BaTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$, $Pb(La,Zr)TiO_3$, $KNbO_3$, $LiNbO_3$ and $PbZrO_3$), have been investigated for a wide variety of electrical and optical applications.

The non - volatile operation of FeRAM is based on the hysteresis characteristics of ferroelectric perovskite materials, such as PZT($Pb(Zr,Ti)O_3$ and SBT ($Sr(Bi,Ta)O_3$). Two stable points at zero electric field, the remanent polarization (± Pr) are used for the non-volatile operation of "0" and "1" states. This is a nonvolatile storage element since the data is present when the voltage is removed. No applied field or voltage is required to maintain the memory, which is why the device is termed "nonvolatile".

Ferroelectric thin films are promise of the important applications such as nonvolatile memory, ferroelectric random access memories,electro - optic waveguide, thin film capacitor, optical modulator, detector, ferroelectric gates (FETs) and metal/insulator/semiconductor transistor device (MIST), metal/ ferroelectric/ semiconductor (MFS) capacitors, metal/ ferroelectric/ insulator/ semiconductor (MFIS) capacitors and ferroelectric memory diode (FMD).

A variety of deposition methods have been proposed for ferroelectric thin films. The methods receiving the most attention are chemical vapor deposition (CVD), sputtering, evaporation, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), sol - gel and metal organic deposition (MOD). They can be divided into dry and wet process. The first five methods are dry processes and are usually required hot substrates. Some of them are relatively slow and expensive but allow greater ease of epitaxial film growth and are still widely used. The last two methods are wet processes and low deposition temperature. They are fast and inexpensive. The ferroelectric thin films are deposited on a variety of substrates including sapphire, silicon, GaAs, fused silica, Pt - coated Al_2O_3, single crystal MgO and $MgAl_2O_4$ and single crystals of several ferroelectrics.

In this paper, the PZT thin films were deposited by thermal evaporation process.Thermal evaporation technique had received considerable attention because of simple and inexpensive method to produce ferroelectric thin film.In this work ,thermal evaporated PZT thin films were fabricated on SiO_2/Si substrates. Physical and elemental analysis was carried out. Ferroelectric properties and switching behaviour of all PZT films were investigated.The aim of the present work is to select the most suitable characteristics of the PZT thin film with various Zr/Ti ratios for FeRAM device.

II. EXPERMENTAL PROCEDURE

The starting materials lead oxide (PbO), titanium oxide (TiO_2) and zirconium oxide (ZrO_2) are mixed in various Zr/Ti ratios and then calcined in the atmosphere. There are four chemical processes, i.e.,

(T< 350ºC) : no reaction;

(350ºC <T< 650ºC) : $PbO + TiO_2 \rightarrow PbTiO_3$;

(650ºC<T<800ºC) : $PbTiO_3 + PbO + ZrO_2 \rightarrow Pb(Zr_{1-x}Ti_x)O_3$;

(800ºC<T<1100ºC): $Pb(Zr_{1-x}Ti_x)O_3 + PbTiO_3 \rightarrow Pb(Zr_{1-x'}Ti_{x'})O_3$; $(x < x')$

Where T is calcined temperature.

Ferroelectric lead ziroconate titanate powder show Ti-rich compositions ($0 \le x \le 0.53$), a tetragonal region whereas compositions with lower Ti-content ($0.53 \le x \le 0.94$), a rhombohedral region. Both regions are separated by a morphotropic phase boundary at x = 0.53. It is clear that the combination reaction of lead zirconate titanate (PZT) powder is essentially completed about 800ºC. To obtain the calcined PZT powder, PbO, ZrO_2 and TiO_2 are mixed in various Zr/Ti ratios and calcined in crucibles at 800ºC for 2h. Prior to the coating, the p-Si (100) substrates (resistivity ρ 1 ~ 15 Ωcm) are cleaned using Standard Cleaning Procedures. Organic and metallic contaminations are removed by etching the solution