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11th **ERDT Conference** on Semiconductor and Electronics, Information and Communications Technology and Energy

16-17 November 2015
Metro Manila, Philippines



**Proceedings of the 8th AUN/SEED-Net RCEEE 2015 and 11th ERDT Conference
on Semiconductor and Electronics, Information and Communications Technology, and Energy**

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ISBN: 978-616-406-075-3

Published by: ASEAN University Network / Southeast Asia Engineering Education Development Network
(AUN/SEED-Net) JICA Project
Faculty of Engineering, Bldg. 2
Chulalongkorn University, Bangkok
Thailand 10330

Printed in the Philippines by: ERZALAN PRINTING PRESS
45 Cotabato Street, Luzviminda Village, Batasan Hills, Quezon City, Philippines

8th AUN/SEED-Net Regional Conference on Electrical and Electronics Engineering 2015

co-located with

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Published by: ASEAN University Network / Southeast Asia Engineering Education
Development Network (AUN/SEED-Net) in partnership with Engineering Research and
Development for Technology (ERDT) and University of the Philippines Diliman.

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Engineering 2015 and 11th ERDT Conference on Semiconductor and Electronics, Information
and Communications Technology, and Energy.

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CMOS DESIGN OF 0.25 μ m CAPACITOR-LESS ALL DIGITAL CONTROLLER FOR A DC-DC BOOST CONVERTER

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ABSTRACT

A purely digital CMOS Design of a controller for a DC-DC Boost converter is presented in this paper using the 0.25 μ m library. The circuit used PWM mode of control. In order to interface the booster analog output to the controller, a time based Analog to digital controller (ADC) is embedded in the design. The ADC also made use of purely digital components. With reference to [1] which used considerable capacitors, the entire design for the booster controller circuit in this paper did not use any capacitor.

Figure 1 shows the general block diagram of the controller. The idea is to have a simple ADC architecture good enough for the booster. A time-based ADC is adopted for the design. The idea of time based ADC was found in [4]. Inside the ADC module is a voltage controlled oscillator (VCO) and a 5 bit counter. Figure 2 shows the general circuitry for the current starved ring oscillator [2] which made it possible to produce the digital output of the ADC by driving the counter at varying frequencies for every sampled output voltage.

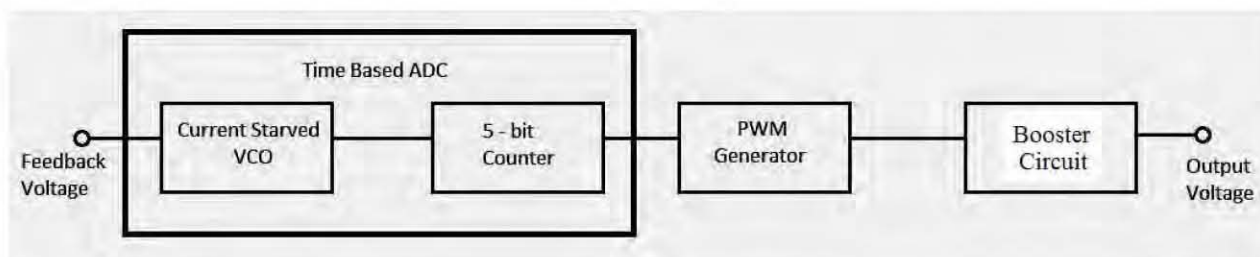


Figure1: General Block Diagram

Because the target output voltage was set at 6V, the power transistor of the main booster circuit made use of another transistor model library. This is because the 0.25 μ m library used for the controller is only limited to a maximum of 2.5V. For the PWM block, it has two main parts, namely the buffer chain and the multiplexer. An input of 150 kHz, originating from the proposed circuit, is being fed to the buffer chain. Each stage of the buffer chain is being tapped to be the input of the 32x1 multiplexer. The output of the multiplexer and the 150 kHz signal is being fed to an XOR which is responsible for yielding the corresponding PWM signal.

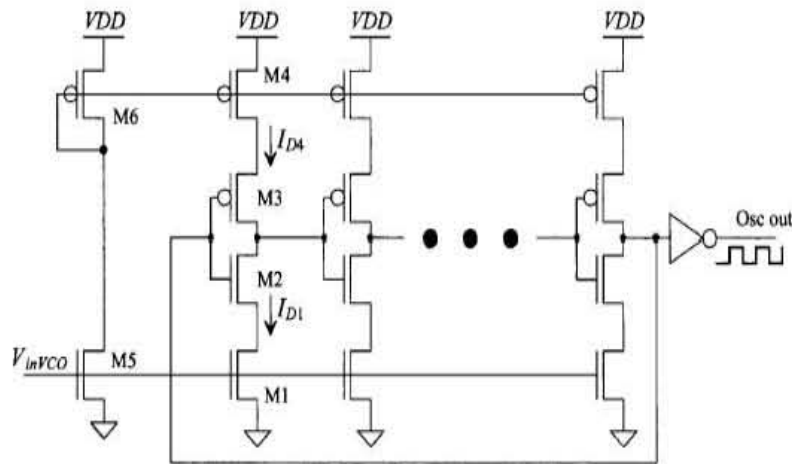


Figure 2: Current Starved Ring Oscillator

Simulation results reveal the booster output stabilizes at 6V for all the corner libraries. Line regulation simulation shows the output is stable for a VDD range of 2.3V to 2.5V. Load regulation simulation reveals the output is maintained at the target voltage of 6V when the load driven is a pair of series connected white LEDs or when the load is replaced by a resistor as low as 100 ohms. The circuit was likewise simulated for temperature variation from 0° to 70°. Data shows the output generally stable close to 6V.

Keywords: current-starved oscillator, capacitor-less, booster

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