Drain and Transfer Characteristics of Al (6 mol %) Doped $PbTiO_3$ Thin Film Transistor

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Abstract **— Al doped $PbTiO_3$ powder was firstly prepared by high temperature solid state reaction route. Structural and microstructural analysis were studied by X-ray diffraction (XRD) and scanning electron microscopy (SEM)). Fabrication process of a single-transistor type ferroelectric field effect transistor (1TFeFET) memory with $PbTi_{(1-x)}Al_{(x)}O_3$ (PTA) films had been carried out. Electrical characteristics (drain & transfer) of all films were measured. According to the experimental results the laboratory-prepared transistors were utilized for 1T of NVFRAM.**

Keywords **— XRD, SEM, 1TFeFET, PTA**

I. INTRODUCTION

Ferroelectric memory FET is of great importance in information technology [1]. Their high speed, nonvolatility, and light weight, combined with low power requirements, physical robustness, and high density, suggested that they would rapidly replace core memories as the nonvolatile memory of choice for most applications[2]. There are many types of memory such as 1T1C type of ferroelectric memory, dynamic random access memory (DRAM), metal/ ferroelectric/ semiconductor (MFS) and metal/ ferroelectric/ insulator/ semiconductor (MFIS), field effect transistor (FET) and ferroelectric random access memory (FeRAM)[3]. 1T1C type of ferroelectric memory has one ferroelectric capacitor and one selective FET per cell. When the read bias is applied to the ferroelectric capacitor selected by FET, the data is detected by the difference in the charge between the switching mode and the nonswitching mode[4].

The ferroelectric memory FET has potentials and nondestructive read out nonvolatile memory with a single transistor per cell like a Flash memory. A metal/ferroelectric/semiconductor (MFS) FET is a typical ferroelectric memory FET. In read operation, the current between the source and drain is sensed. The ferroelectric polarization does not reverse and the data is not destroyed in the read operation. However, fabrication of a conventional (MFS)FET is very difficult because of deposition the ferroelectric film directly on Si. To realize the ferroelectric memory FET for practical use, a metal/ferroelectric/metal/ insulator/semiconductor (MFMIS)FET. By inserting an insulator such as MgO, CeO_2, ZrO_2, TiO_2, $PbTiO_3$ a MFS FET changes into a MFIS FET. Because it improves on the current technologies, it presents itself as the ideal candidate for a future generation universal type of memory [5]. In this paper, electric characteristic of PTA films were described.

II. EXPERIMENTAL PROCEDURE

The properties of the solid solution were strongly influenced by their preparation procedure. To prepare the sol-gel precursor solution, PbO, TiO_2 and Al_2O_3 were used as starting materials. The purity of materials was 99.9% as analar grade. Each of these three materials was grinded in agate mortar for three hours to form homogeneous grain size. To reduce the grain size, the powder was sieved with 3-stages mesh sieve (100 mesh , 250 mesh and 400 mesh). Then this sample powder was dispersed by the air-jet milling under the pressure of 40 lb/in^2 to obtain the moisture less particle and blander for 15 minutes with constant pressure to ensure good dispersion. And then the powder was grinded by ball-milling in 20 hours. Then they were mixed to get the chemical formula $PbTi_{(1-x)}Al_xO_3$ (x=0.06mol%) powder. And then it was heated on 800°C and 900°C for 1 hour. The PTA powder (900°C) was chosen for further investigation because of its smaller crystallite size. Al doped $PbTiO_3$ were weighted and dissolved in 2 methoxyethanol solvent. The mixture solution was acidified with 3mg of HCl. The solution was stirred and refluxed up to obtain precursor solution.

The substrate used for this study was p-Si(100), which were (0.5cm×1cm) and thickness of 280-300μm. Before film fabrication, they were washed ultrasonically in distilled water. Then they were washed in boiling acetone and in boiled propenol for 5 minutes to remove greasy films. And then they were immersed in nitric acid for 5 minutes in order to remove ionic contamination. After that they were etched in buffered hydrofluoric acid for 5 minutes to remove oxide films. Finally the Si wafers were cleaned in distilled water and dried on flat oven at 100°C in open air for a few minutes then the cleaned Si wafers were obtained.

SiO_2, as an insulating layer, was thermally deposited on p-Si (100) by heating at 1200°C into the furnace about 1 hour. The middle zone of SiO_2/Si structure was covered with apiezon wax and the remaining zones were etched with
HF: DI water (1:3) to remove SiO_2 layer totally. To fabricate source (S) and drain (D) regions, n type phosphorus was deposited on these layers and annealed at 550°C for 1 hour. By diffusion mechanism, S and D regions were obtained at

the ends. And then, the precursor solution was deposited on middle zone of SiO_2 layer using spin coating to get gate region. The three process temperatures (500°C, 600°C and 700°C) were also performed according to examine the PTA film quality at different annealing temperature. Fig 1 showed fabrication and deposition procedure of MFIS field effect transistor.

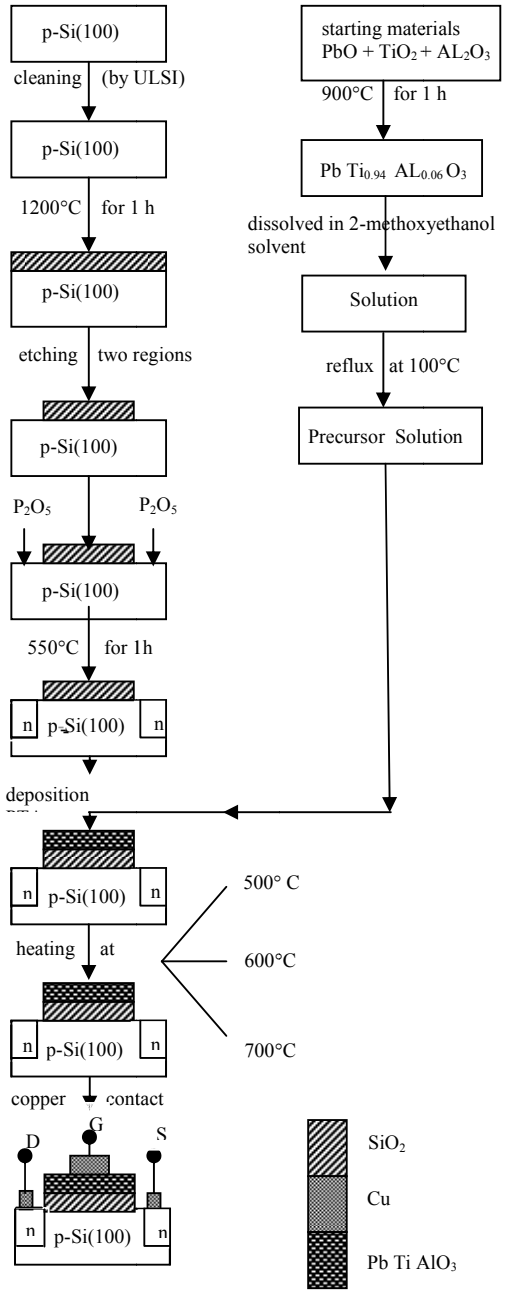

Fig 1 Fabrication and deposition procedure of FeFET

III. RESULTS AND DISCUSSION

A. XRD Analysis

The information about the crystallographic properties such as crystallite size and lattice parametres of the samples had been obtained from the XRD profiles. The XRD spectra of $PbTiAlO_3$ powder with different reaction temperatures at 800°C and 900°C were shown in Fig 2(a&b). As shown in Fig ,the XRD spectrum of PTA powder graphs were produced within the diffraction angle range from 10° to 70°.The dominant peaks were formed at(101) plane with 2 θ of 31.90° and 31.96° respectively. The lattice parameters, FWHM, and crystallite size (G) were listed in Table 1. From XRD profiles, perovskite type, pure $PbTiO_3$ structures were formed.

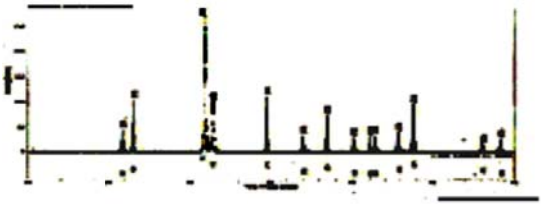

Fig2(a) XRD pattern of $PbTiAlO_3$ powder, process temperature at 800°C

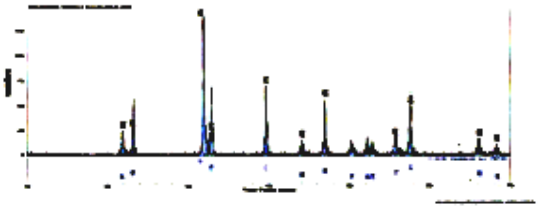

Fig 2(b) XRD pattern of $PbTiAlO_3$ powder, process temperature at 900°C

TAABLE I
STRUCTURAL PROPERTIES OF $PBTIALO_3$ POWDER

Process Temperature	800°C	900°C
a - axis(Å)	3.8559	3.8559
c - axis(Å)	4.0703	4.0693
c/a	1.0556	1.0556
FWHM (rad)	2.69E-3	4.05E-3
Crystallite size (nm)	52.5	38.8

B. SEM Analysis

SEM investigation was performed to study the grain morphology of PTA powder at different annealing temperatures. Fig 3 (a & b) showed the SEM image of PTA powder at 800°C and 900°C. The powder was composed by spherical shaped densely packed particles. The grain arrangement was seen to be uniform and crack free. The grain-

size of PTA powder was estimated to be 0.643 μm at 800°C and 0.5 μ m at 900°C.

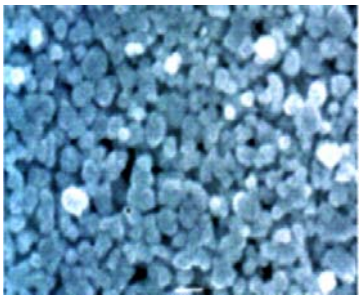

Fig 3(a) SEM image of $PbTiAlO_3$ powder, process temperature at 800°C

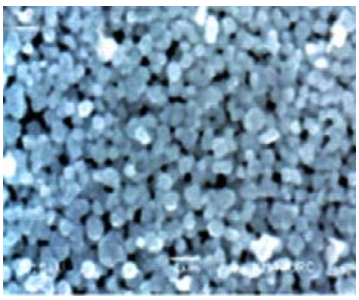

Fig 3(b) SEM image of $PbTiAlO_3$ powder, process temperature at 900°C

C. Output Characteristics

To examine the output characteristics of fabricated transistor, I_{DS}-V_{DS} variation (drain characteristics) was measured at different gate to source voltages. The experimental circuit diagram and circuit diagram were shown in Fig 4(a&b) . The characteristic curves were displayed at Fig 5(a-c). From the figure, it was found that two different regions such as linear and saturation were observed.

At low drain voltage, between 0V to 4V, the drain current increased linearly with increase in drain voltages. In this region, the FET exhibited a resistive characteristics with the resistance as a function of the gate voltage. The drain current I_D increased with increase in drain voltage V_D and become saturated at the pinch-off point. After that, the I_D did not increase whereas increased in drain voltage V_D, which showed saturated or constant region.

Moreover, the drain current was also enhanced with increasing gate voltages. So fabricated transistor was only operated in E-mode (enhancement-mode).

From drain characteristic curve, the drain current did not allowed to flow when the drain voltage approached zero. On the other hand, the drain current was zero if zero-bias gate voltage was applied. These facts showed the fabricated FeFET had normally- off nature.

To examine the device quality, (I_{DS}-V_{GS} variation), transfer characteristics were essentially observed at saturation-mode. These graphs were shown in Fig 6(a-c). From the figure, it was seen that the I_{DS} was exponentially increased with gate voltage.

All transfer curves were varied gate potential with threshold voltage. All threshold voltages were found to be temperature influence and these were listed in Table.2.

The largest maximum drain current was caused by the cell at 700°C. To check the parabolic nature of transfer curve (or) the I_{DS} and (V_{GS} -V_{TH}) variation, m^{th} power of (V_{GS} -V_{TH}) was essentially studied by two unknown equations

$$I_{DS} = K (V_{GS}-V_{TH})^m$$

Where I_{DS}= drain current

K = constant

V_{GS}= gate to source voltage

V_{TH}= threshold voltage

At V_{GS} = 6V, V_{TH} = 3.44 V, I_{DS} = 5.6 μA

V_{GS} = 7V, V_{TH} = 3.44 V, I_{DS} = 11 μA

$$5.6 = K (6 - 3.44)^m \quad (1)$$

$$11 = K (7 - 3.44)^m \quad (2)$$

Eqn (2) / (1), m =2.04 for the cell at 500°C. The m^{th} power values were collected in Table.2.

To identify the transconductance value, $I_D^{1/m}$ was characterized with V_{GS} and shown in Fig.7 (a-c). From the characteristic curve, $I_D^{1/m}$ was linearly enhanced when the gate to source voltage was increased. The slope gave its transconductance value. The g_m value was measured by equation $g_m=\Delta I_D / \Delta V_{GS}$.A large transconductance was desirable to minimize the gate drive and provided high power gain. These values were organized and quoted in Table 2.

TABLE II
V_{TH}, $I_{D,MAX}$, M^{TH} POWER AND G_M AT DIFFERENT PROCESS TEMPERATURES

Process Temperature	500°C	600°C	700°C
V_{TH}(V)	3.44	3.33	4.33
I_{Dmax}(μA)	0.57	0.88	1.37
m^{th} power	2.04	1.95	2.11
g_m(μS)	1.7561	1.4853	2.4405

Fig 4(a) The experimental circuit diagram of FeFET for drain characteristics

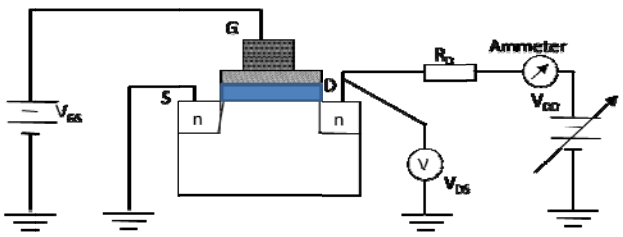

Fig 4(b) The circuit diagram of FeFET for drain characteristics

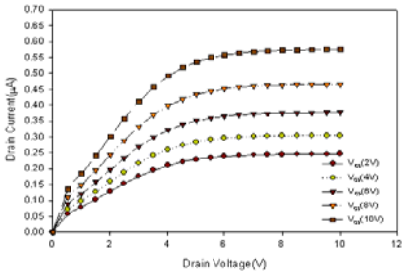

Fig 5 (a) Drain characteristic of PTA-gated FET at 500°C.

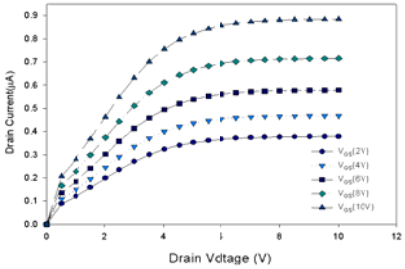

Fig 5 (b) Drain characteristic of PTA-gated FET at 600°C.

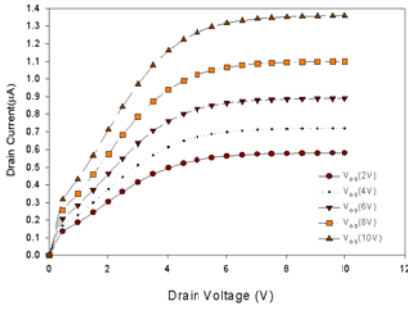

Fig 5 (c) Drain characteristic of PTA-gated FET at 700°C.

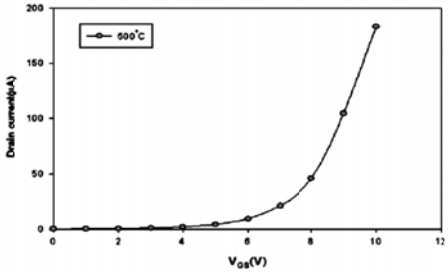

Fig 6 (a) Transfer characteristics of PTA-gated FET at 500°C

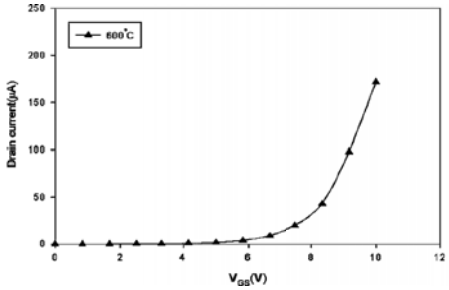

Fig 6 (b) Transfer characteristics of PTA-gated FET at 600°C

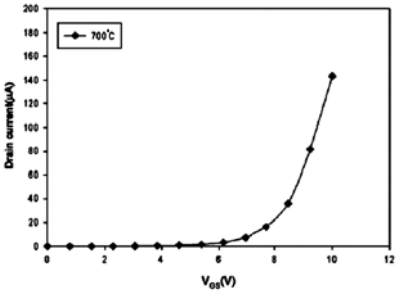

Fig 6 (c) Transfer characteristics of PTA-gated FET at 700°C

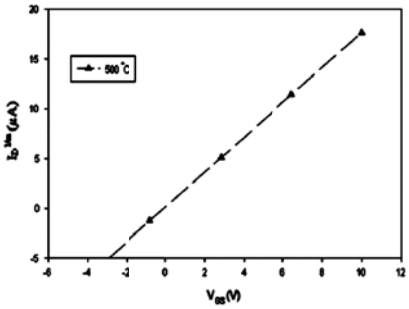

Fig 7 (a) Transconductance characteristics of PTA gated FET at 500°C in saturation mode.

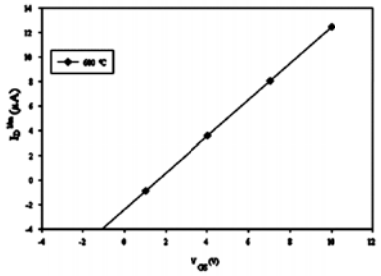

Fig 7 (b) Transconductance characteristics of PTA gated FET at 600°C in saturation mode.

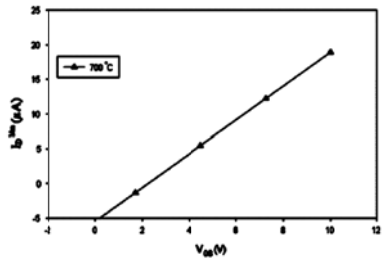

Fig 7 (c) Transconductance characteristics of PTA gated FET at 700°C in saturation mode.

IV. CONCLUSION

Fabrication of PTA 6 gated FET and its output characteristics had been studied. According to the experimental results, salient conclusions were made as follows. The fabricated cells were only operated in E-mode. The normally-off nature of fabricated cells was found on drain characteristic curve too.

From transfer characteristics, I_{DS} and V_{GS} graph was found to be parabolic nature as $I_{DS} = K (V_{GS}-V_{TH})^2$. $I_D^{1/m}$ and V_{GS} graph was examined to be linear relationship. The measurement m^{th} power values were ranged from 1.95 to 2.11. This fact gave the parabolic nature of transfer curve for fabricated cells. The slope of $I_D^{1/m}$ - V_{GS} graph gave the transconductance value of fabricated cells. According to the experimental results such as threshold voltage, m^{th} power, and transconductance values, the laboratory-prepared transistor can be utilized for 1T of NVFRAM.

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REFERENCES

[1] Iijima K et al, 1986,J Appl Phys, 60 361
[2] Carlos A et al, 1990, Ferroelectrics, 104 241
[3] Willian A et al, 1991, IEEE Transcations on Ultrasonics, 18 704
[4] Hwang Y et al,1998,Jpn J Appl Phys,37 1332
[5] Tyagi M S, 1991, "Introduction to Semiconductor Materials and Devices". (New Delli:Wiley)