ICSE 2009

PROCEEDINGS OF THE FIRST INTERNATIONAL CONFERENCE ON SCIENCE AND ENGINEERING

Volume - 1

Electronics
Electrical Power
Information Technology
Engineering Physics

Sedona Hotel, Yangon, Myanmar
December 4-5, 2009

PROCEEDINGS OF THE FIRST INTERNATIONAL CONFERENCE ON SCIENCE AND ENGINEERING

Volume - 1

Electronics
Electrical Power
Information Technology
Engineering Physics

Organized by
Ministry of Science and Technology

DECEMBER 4-5, 2009

SEDONA HOTEL, YANGON, MYANMAR

ELECTRONIC ENGINEERING

Silicon Backplane Design for OLED-on-silicon Microdisplay

Ying Wang[#1]

[#]*School of Electrical and Electronic Engineering, Nanyang Technological University*
50 Nanyang Avenue, Singapore 639798
[1]wangying@ntu.edu.sg

***Abstract*—The silicon backplane of the 160×120 OLED-on-silicon microdisplay is proposed using Semiconductor Manufacturing International (Shanghai) Corporation (SMIC) 0.35µm custom silicon process. Current driving scheme is developed owning to the simplification and integration of this kind of pixel circuit architecture. To decrease the driving frequency, line-at-a-time refresh mode is implemented with the integrated data buffer. 16 levels gray scales are achieved employing a current mode digital to analog converter (DAC). A top emit structure of OLED device is developed for OLED-on-silicon microdisplay.**

***Keywords*—OLED, microdispay, silicon backplabe, current driving scheme, line-at-a-time refresh mode**

I. INTRODUCTION

Organic Light Emitting Diode (OLED), since its first observation of light emission in small molecules based LEDs by Tang *et al.* and conjugated polymer LEDs by Burroughes *et al.*, there has been a continuous and rapid improvement in device performance.

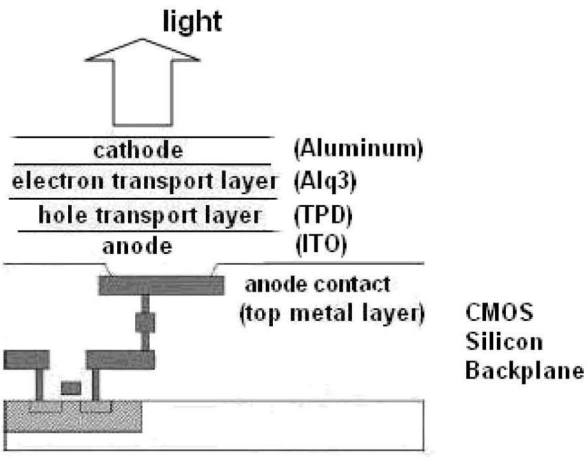


Fig. 1 The structure of OLED-on-Silicon microdisplay

Improvements in areas such as efficiency, stability and full color tuning have enabled OLED based products to reach the market and compete with the existing technologies, especially in the area of flat panel displays. It is challenging the liquid crystal display as an alternative technology by the strength in ease of manufacturing and all solid-state nature. Moreover it also features in wide viewing angle, short response time, large contrast ratio, good color reproduction, wide temperature range operation, *etc.* Combined with CMOS technology, the OLED device can be deposited on the silicon backplane to provide high optical performance and low power dissipation. The proposed OLED-on-Silicon microdisplay is shown in Fig. 1 and a top emit structure is used due to the opaque silicon substrate. In our design, the top metal layer of the CMOS process is used as the contactor of the Indium Tin Oxide (ITO) anode for the OLED devices. Hole transporting layer of TPD and the electron transporting layer using Alq3 are deposited on this ITO coated CMOS silicon backplane. A transparent aluminium layer is deposited on the top to form the cathode.

II. CIRCUIT IMPLEMENTATION

The 160×120 OLED microdisplay silicon backplane has implemented and under fabrication with the SMIC 0.35µm 3.5V/5.0V CMOS process. The whole area of this circuitry is 10mm×8mm with the pixel size of 50µm×50µm. The function block of the design is shown below in Fig. 2.

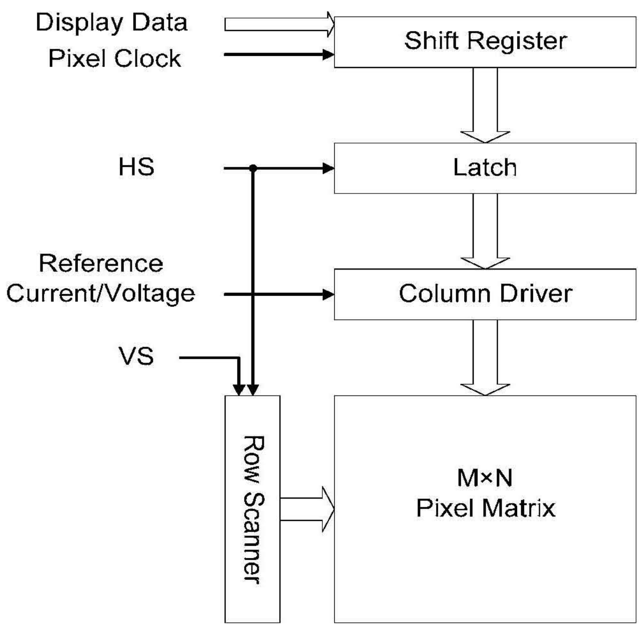
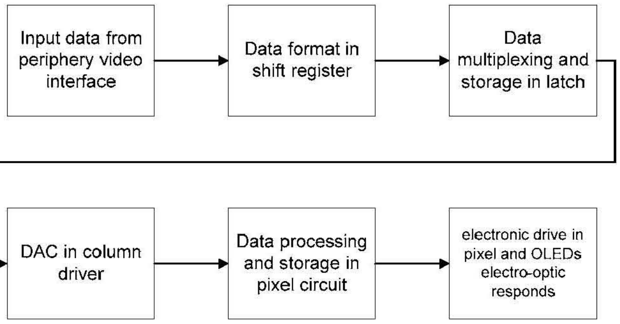


Fig. 2 Function blocks of OLED-on-silicon silicon backplane

A. Addressing Circuit

The input signals' data path through OLED-on-Silicon microdisplay and the timing schedule are illuminated in Fig. 3 and Fig. 4. The input data is sorted, stored at shift register and data latch and converted from digital to analog format by the a current mode DAC in the column driver. The analog display data is written to the column data line connected to the pixel circuit. The analog data is stored and may be further processed at the pixel where the electro-optical responds of OLEDs happens.



Fi

Fig. 3 Data path of OLED-on-Silicon Microdisplay

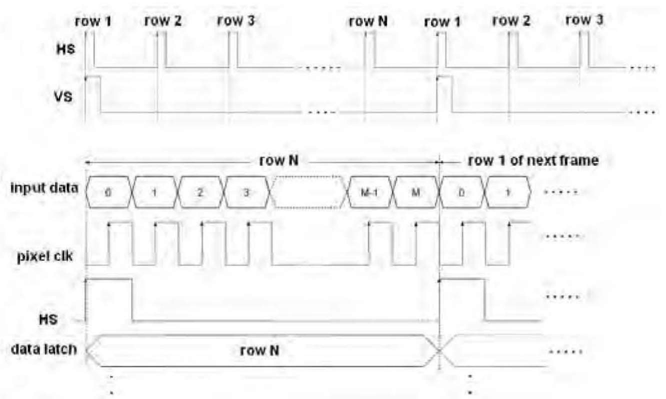


Fig. 4 Timing schedule of input signals

The structure shift register, data latch are shown in Fig. 5. The input 4 bit data will be transferred into the shift register by the pixel clock. The shift register works as a serial-to-parallel converter. The data of a whole row will be stored in the data latch first then under the control of the horizontal synchronization signal (HS), the data are loaded to the DAC for further performance.

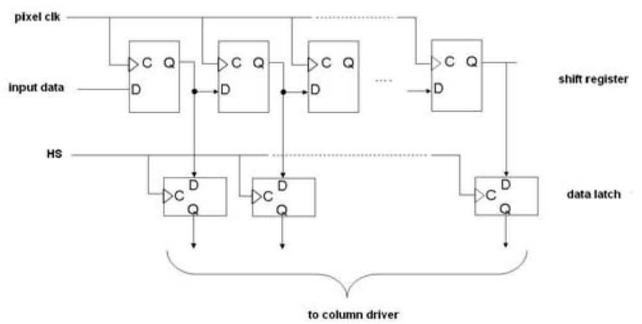


Fig. 5 Structure of shift register and data latch

The schematic of the row scanner is shown in Fig. 6. The row scanner consists of N D-flip/flops to form a shift register clocked by the HS signal. The display row is enabled line by line when the row selection signal is shifted in the row scanner to realize a line-at-a-time refresh mode. The whole scan motion will repeat at the raising edge of vertical syncretisation signal (VS).

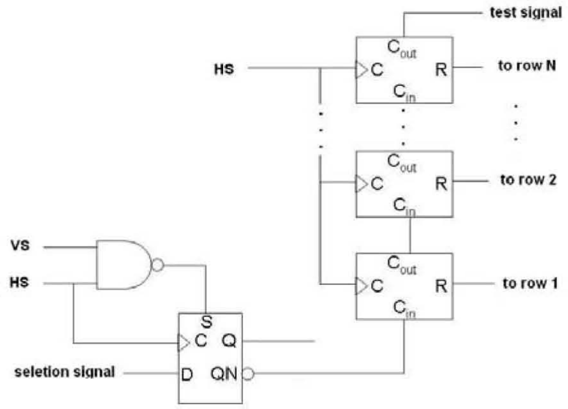


Fig. 6 The schematic of the row scanner

B. Pixel Circuit

Two approaches can be used to modulate the OLED display. Selection is between the current voltage driving and current driving. Since the luminance of an OLED is proportional to its current density, current mode driving circuit is the natural choice for OLED microdisplay. Current driving pixel circuit is shown in Fig. 7.

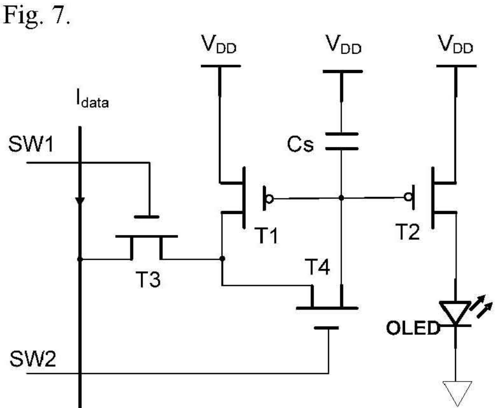


Fig. 7 Current driving pixel circuit

A current mirror is the basic component of such pixel circuit structure. The data current I_{data} will be converted to a certain value of gate voltage of T1 stored across Cs during the programming period and in the emission period such driving current I_{data} will be copied to OLED devices with the current mirror pair of T1 and T2. The advantage of current mirror structure is by adjusting the (W/L) ratio of current mirror pair, large value of data current I_{data} can be used in the programming period in order to improve the accuracy and shorten the programming time. In practical, the dimensions of T1 and T2 are design as $(W/L)_{T1} = (W/L)_{T2}$, where k is larger than 1. The data current I_{data} is shrunk in order to provide a proper OLED current I_{OLED} according to the factor k.

The simulation results of pixel circuit are shown in Fig. 8. From the results, we find that only when the row selection signal SW1=SW2=HIGH is valid, the current display data from DAC will be transferred into pixel circuit and injected into the OLED device to illuminate the display.

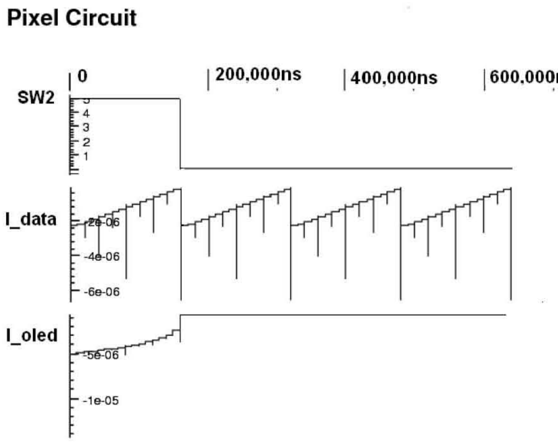


Fig. 8 Simulation results of pixel circuit

C. Current-Mode DAC

To provide proper designed current display data to the pixel circuit, a cascaded current DAC is employed integrated in column driver. For OLED-on-Silicon microdisplay, very tight area constraint is on the current DAC for each column drivers, especially with the increase of the display pixel density for the microdisplay with high resolution.

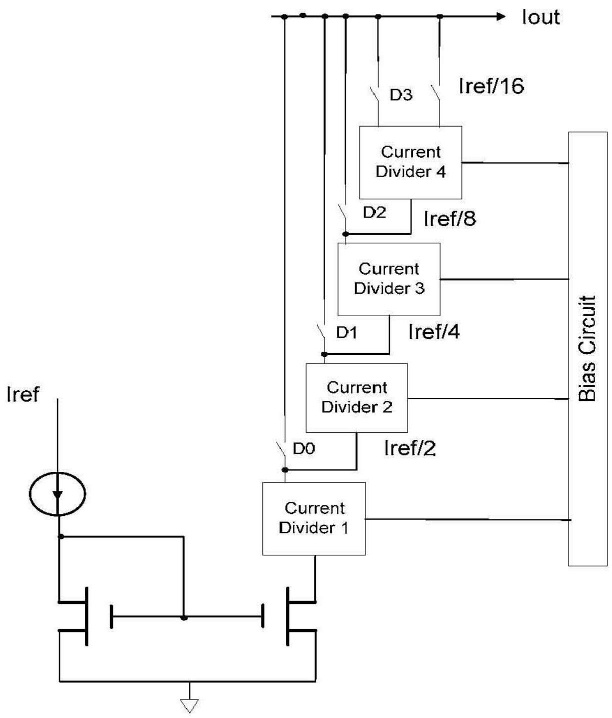


Fig. 9 (a)

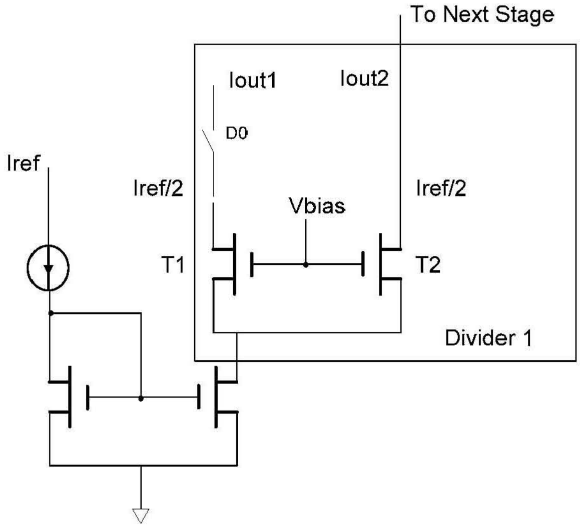


Fig. 9 (b)

Fig. 9 (a) Architecture of 4 bit current mode DAC
(b) Architecture of current divider

The basic architecture of 4-bit cascaded current DAC is illuminated in Fig. 9 (a). The current dividers (shown in Fig. 9(b)) can divide the current I_{ref} into two equal current flows. The current mirror is used as the current divider. If the matching between T1 and T2 is sufficient, the two currents I_{out1} and I_{out2} are equal to each other, $I_{ref}/2$.

The I-V characteristics of OLED are similar to a p-n junction diode. The typical I-V characteristic curve of the OLED device developed in our research is shown below in Fig. 10.

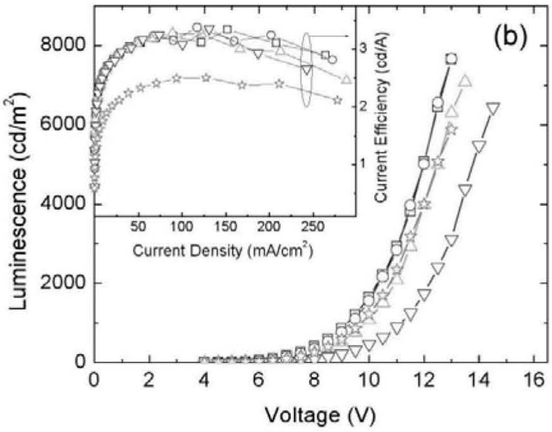


Fig. 10 The I-V curve of OLED device developed in our research group

We aim to achieve the display luminescence of 300 cd/m^2 – 3000 cd/m^2 for our OLED-on-silicon microdisplay. According to the I-V curve, the current efficient is around 3 cd/A, so the current density will be 10 mA/cm^2 – 100 mA/cm^2. With the pixel size of 50μm×50 μm, the driving current should be ranging from 250nA to 2500nA.

The 4 bit DAC simulation result is shown in Fig. 11.When the pixel circuit turns ON, the range of the pixel driving current is from 2500nA to 250nA with the change of the data current.

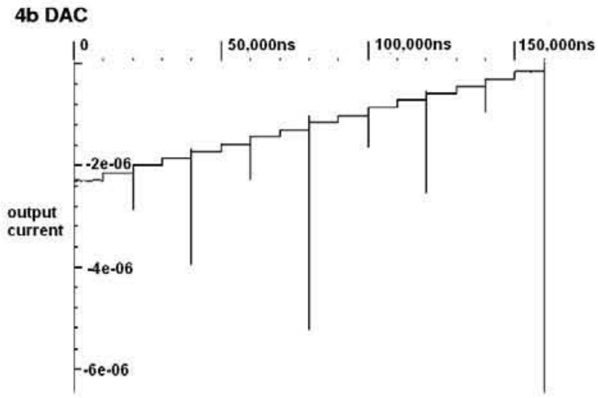


Fig. 11 Current mode DAC simulation result

The INL and DNL of this current mode DAC are shown in Fig. 12 (a) and 12 (b).

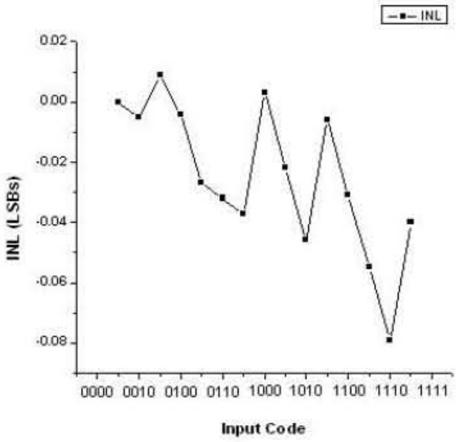


Fig. 12 (a)

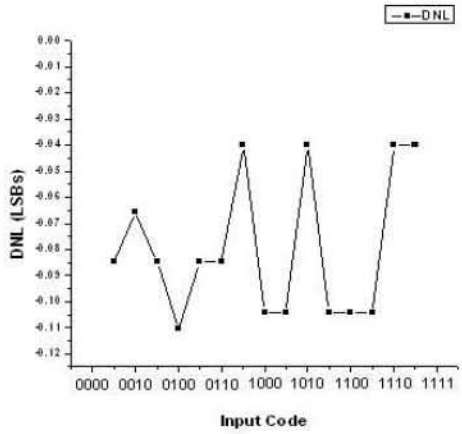


Fig. 12 (b)

Fig. 12 (a) INL of 4 bit current mode DAC
(b) DNL of 4 bit current mode DAC

Table I summarizes the simulation results for the 4 bit current mode DAC. The current mode DAC achieves good INL and DNL performances. The simulation results show the proposed DAC can properly work as we designed.

TABLE I

SUMMARY OF DAC SIMULATION RESULTS

Technology	SMIC 0.35μm 3.5V/5.0V CMOS process
Resolution	4 bit
Power Supply	5V
Power Dissipation	12.5μW(IDAC,OUT, MAX=2.5 μA)
INL	-0.08LSB (worst case)
DNL	-0.11LSB (worst case)

III. Conclusion

The specifications of the proposed silicon backplane of OLED-on-silicon microdisplay are list in Table II.

TABLE II

SPECIFICATIONS OF 160×120 OLED-ON-SILICON MICRPDISPLAY

Technology	SMIC 0.35μm 3.3V/5.0V CMOS process
Die size	8mm×6mm
Resolution	160×120
Pixel Size	50 μ m×50 μ m
Driving Scheme	Current Driving
Frame Rate	60Hz (VGA video signals)
Pixel Clock Rate	1.152MHz
Gray Scale Levels	16 levels

The 160 × 120 OLED-on-Silicon microdisplay is developed in current driving scheme, which supports 16 grey levels display. The circuit design of main function blocks is presented in detail descriptions. This scheme makes it possible to implement the microdisplay application with OLED display technology.

References

[1] C. W. Tang and S. A. Van Slike, "Organic electroluminescent diodes," Appl. Phys. Lett., vol. 51, pp. 913–915, 1987.

[2] J. H. Burroughes, D. D. C. Bradley, A. R. Brown, R. N. Marks, K. Mackay, R. H. Friend, P. L. Burns, and A. B. Holmes, "Light-emitting diodes based on conjugated polymers, " Nature, vol. 347, pp. 539–541,1990.

[3] N. K. Patel, S. Cinà, and J. H. Burroughes, "High-Efficiency Organic Light-Emitting Diodes, " IEEE Journal on Selected Topics in Quantum Electronics, vol.8, pp: 346-361, 2002.

[4] G. B. Levy, W. Evans, J. Ebner, P. Farrell, M. Hufford, B. H. Allison, D. Wheeler, H. Q. Lin, O. Prache, and E. Naviasky, "An 852 x 600 pixel OLED-on-silicon color microdisplay using CMOS subthreshold-voltage-scaling current drivers," Ieee Journal of Solid-State Circuits, vol. 37, pp. 1879-1889, Dec 2002.

[5] O. Prache, "Full-color SVGA+ OLED-on-silicon microdisplay," Journal of the SID, vol. 10, pp. 133-138, 2002.

[6] Y. Divayana, B. J. Chen, X. W. Sun, and K. S. Sarma, "Organic light-emitting devices with a hole-blocking layer inserted between the hole-injection layer and hole-transporting layer," Applied Physics Letters, vol. 88, Feb 2006.